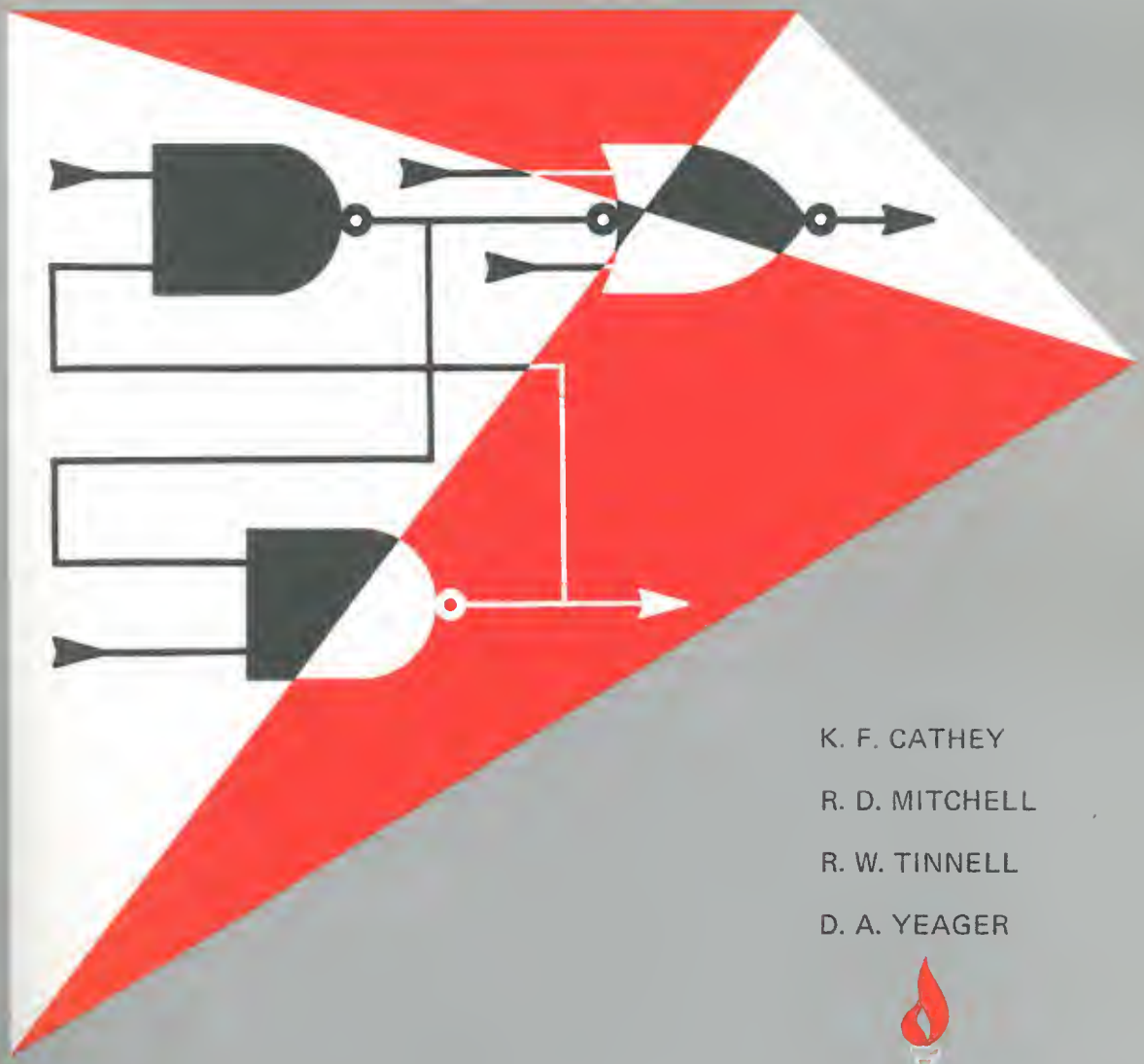
ELECTRONICS

DIGITAL



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Foreword

The marriage of electronics and technology is creating new demands for technical personnel in today's industries. New occupations have emerged with combination skill requirements well beyond the capability of many technical specialists. Increasingly, technicians who work with systems and devices of many kinds — mechanical, hydraulic, pneumatic, thermal, and optical — must be competent also in electronics. This need for combination skills is especially significant for the youngster who is preparing for a career in industrial technology.

This manual is one of a series of closely related publications designed for students who want the broadest possible introduction to technical occupations. The most effective use of these manuals is as combination textbook-laboratory guides for a full-time, post-secondary school study program that provides parallel and concurrent courses in electronics, mechanics, physics, mathematics, technical writing, and electromechanical applications.

A unique feature of the manuals in this series is the close correlation of technical laboratory study with mathematics and physics concepts. Each topic is studied by use of practical examples using modern industrial applications. The reinforcement obtained from multiple applications of the concepts has been shown to be extremely effective, especially for students with widely diverse educational backgrounds. Experience has shown that typical junior college or technical school students can make satisfactory progress in a well-coordinated program using these manuals as the primary instructional material.

School administrators will be interested in the potential of these manuals to support a common first-year core of studies for two-year programs in such fields as: instrumentation, automation, mechanical design, or quality assurance. This form of *technical core* program has the advantage of reducing instructional costs without the corresponding decrease in holding power so frequently found in general core programs.

This manual, along with the others in the series, is the result of six years of research and development by the *Technical Education Research Centers, Inc.*, (TERC), a national nonprofit, public service corporation with headquarters in Cambridge, Massachusetts. It has undergone a number of revisions as a direct result of experience gained with students in technical schools and community colleges throughout the country.

Maurice W. Roney

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Preface

Technology, by its very nature, is a laboratory-oriented activity. As such, the laboratory portion of any technology program is vitally important. *Electronics/Digital* is intended to provide meaningful experience in digital circuit analysis for students of modern technology.

The topics included provide exposure to: basic principles of digital logic, logic gates, flip-flops and other circuits, as well as to basic digital systems.

The sequence of presentation chosen is by no means inflexible. It is expected that individual instructors may choose to use the materials in other than the given sequence.

The particular topics chosen for inclusion in this volume were selected primarily for convenience and economy of materials. Some instructors may wish to omit some of the exercises or to supplement some of them to better meet their local needs.

The materials are presented in an action oriented format combining many of the features normally found in a textbook with those usually associated with laboratory manual. Each experiment contains:

1. An INTRODUCTION which identifies the topic to be examined and often includes a rationale for doing the exercise.
2. A DISCUSSION which presents the background, theory, or techniques needed to carry out the exercise.
3. A MATERIALS list which identifies all of the items needed in the laboratory experiment. (Items usually supplied by the student such as pencil and paper are not normally included in the lists.)
4. A PROCEDURE which presents step-by-step instructions for performing the experiment. In most instances the measurements are done before calculations so that all of the students can at least finish making the measurements before the laboratory period ends.
5. An ANALYSIS GUIDE which offers suggestions as to how the student might approach interpretation of the data in order to draw conclusions from it.
6. PROBLEMS are included for the purpose of reviewing and reinforcing the points covered in the exercise. The problems may be of the numerical solution type or simply questions about the exercise.

Students should be encouraged to study the text material, perform the experiment, work the review problems, and submit a technical report on each topic. Following this pattern, the student can acquire an understanding of, and skill with, basic digital circuits that will be extremely valuable on the job.

These materials on digital electronics comprise one of a series of volumes prepared for technical students by the TERC EMT staff at Oklahoma State University, under the direction of D.S. Phillips and R.W. Tinnell. The principal authors of these materials were K.F. Cathey, R.D. Mitchell, R.W. Tinnell and D.A. Yeager.

An *Instructor's Data Guide* is available for use with this volume. Mr. Kenneth F. Cathey was responsible for testing the materials and compiling the instructor's data book for them. Other members of the TERC staff made valuable contributions in the form of criticisms, corrections, and suggestions.

It is sincerely hoped that this volume as well as the other volumes in this series, the instructor's data books, and the other supplementary materials will make the study of technology interesting and rewarding for both students and teachers.

THE TERC EMT STAFF

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experiment 00001 BINARY NUMBER SYSTEM

INTRODUCTION. In order to facilitate high-speed calculations in digital computers, new machine languages can be used. In this experiment we will examine the Binary Number System and perform some arithmetic operations using this system of numbers.

DISCUSSION. *Binary arithmetic* is the "machine language" of many computers. A good knowledge of computer fundamentals can open many rewarding career opportunities. A digital computer can operate at very high speeds. It uses basically only two conditions, "off" and "on". These two conditions can be translated to the characters 0 and 1, which are the two digits of the Binary Number System. The computer works with these two binary numbers, and all information to be used inside the machine must be converted into binary numbers. You will need to know this machine language to understand computer operations.

Since the machines we are discussing are made up of devices that respond to only two states, we need to develop a number system to match. That is to say, our usual number system will not work with such a machine because it employs ten digits.

We all know that our everyday number system has only ten digits and that all other numbers in the system are made up of combinations of these digits. We don't usually think of 465 as being made up of four hundreds (10 times 10), six tens (10 times 1), and five units (10 times 0.1). The number 10 is called the base of the decimal system. It is *NOT* a basic digit in the system. In this system (or any worthwhile number system), a number is said to have position. This makes 071 mean zero hundreds, seven tens and one unit, while 710 means seven hundreds, one ten, and zero units. The position of the digits determines the magnitude of the number.

The number 524 can be read five hundreds, two tens, and four units. It could also be expressed:

$$524 = 5 \times 10^2 + 2 \times 10^1 + 4 \times 10^0$$

$$(10^0 = 1) \qquad (1.1)$$

So

$$524 = 5 \times 100 + 2 \times 10 + 4 \times 1$$

$$524 = 500 + 20 + 4$$

$$524 = 524$$

The *base* of the number system is the number which, when raised to the zeroth power gives the lowest position value, and when raised to the first power, it is the second position, etc. We can write the general equation for any number system as:

$$N = R^n d_n + \ldots + R^3 d_3 + R^2 d_2 + R^1 d_1 + R^0 d_0 \qquad (1.2)$$

where:

N = the number

d_n = the digit in that position

R = the *radix* (base of the system)

Substituting:

$$5654 = 5 \times 10^3 + 6 \times 10^2 + 5 \times 10^1 + 4 \times 10^0$$

$$5654 = 5000 + 600 + 50 + 4$$

$$5654 = 5654$$

So much for the number system we are familiar with. It can be difficult and time-consuming for a computer to handle a ten-digit number system in its millions of computations due to its ability to add many numbers with fewer digits. For this reason the Binary Number System is often employed.

The binary system has only two digits, 0 and 1. Let's test the binary (base 2) system against our general equation to see if it produces different numbers in each position. $2^0 = 1$ and $2^1 = 2$, etc., which satisfies the definition. Why couldn't the base be 0? Again, applying the rule we can see that a base 0 system probably isn't very useful because $0^0 = 1$ and $0^1 = 0$ as does 0 to any power. The base 1 system is similar to a base zero system. It has only one digit since multiplying one by itself any number of times produces only one. Thus, this system too is not very useful. Consequently the binary (base 2) system is the simplest usable system. It contains only two digits but can express any number with these digits.

A comparison of the base 2 and base 10 systems (see Fig. 1-1) may be helpful.

The binary system has only two digits and all numbers are constructed with them. The general definition (1.2) applies to the system and can be simplified to

$$N = \ldots + 8d_3 + 4d_2 + 2d_1 + 1d_0 \quad (1.3)$$

The digits in this equation (d_0, d_1, d_2, d_3) are either 0 or 1. If

N = 11011 in binary then

$N = 1 \times 16 + 1 \times 8 + 0 \times 4 + 1 \times 2 + 1 \times 1$

$N = 16 + 8 + 0 + 2 + 1$

N = 27 in decimal

or,

$N = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$N = 1 \times 16 + 1 \times 8 + 0 \times 4 + 1 \times 2 + 1$

$N = 16 + 8 + 0 + 2 + 1$

N = 27

For instructional purposes these numbers have been expressed in the familiar decimal system. We can convert to binary notation in order to take advantage of the simpler digits.

Figure 1-2 shows the decimal digits expressed in binary code.

From equation 1.3 for the base two number system, we have evolved

$$N = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$

which is the decimal number 27 expressed in the binary form. By further inspection the binary form of the number 27 can be reached. You will notice that each of the multipliers for the powered numbers in the equation are either 0 or 1. These digits tell whether or not the particular position is filled in the binary

Base 10		Base 2	
$10^0 = 1$	Units	$2^0 = 1$	Units
$10^1 = 10$	Tens	$2^1 = 2$	Twos
$10^2 = 100$	Hundreds	$2^2 = 4$	Fours
$10^3 = 1000$	Thousands	$2^3 = 8$	Eights
$10^4 = 10{,}000$	Ten Thousands	$2^4 = 16$	Sixteens

Fig. 1-1 Base Ten — Base Two Comparison

Decimal	Binary
0	0
1	1 (1×2^0)
2	10 ($1 \times 2^1 + 0 \times 2^0$)
3	11 ($1 \times 2^1 + 1 \times 2^0$)
4	100 ($1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$)
5	101 ($1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$)
6	110 ($1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$)
7	111 ($1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$)
8	1000 ($1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$)
9	1001 ($1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$)

Fig. 1-2 Decimal Digits Expressed in Binary

system. In other words, when the ones appear it says, "Yes, this position is filled for this number." Therefore, the binary notation for the decimal number 27 is 11011. It has 1 power 2^4, plus 1 power 2^3, plus 0 power 2^2 plus 1 power 2^1, plus 1 power 2^0 or "yes, yes, no, yes, yes." This corresponds well with the "on", "off" capability of devices from which computers are made.

We can get decimal numbers from binary numbers but how do we get binary numbers from decimal numbers? The procedure is quite easy and takes longer to explain than to learn. It consists of successive divisions by the base number. The base will *either* go into the number evenly, *or* have a remainder of one. The presence of the remainder determines whether or not that power position is filled. For instance, if we desire to write the binary form of $(25)_{10}$ (which is read as twenty-five, base 10), first divide the number by two:

Remainder

25 divided by 2 = 12 + 1
Then divide 12 by 2 = 6 + 0
Then divide 6 by 2 = 3 + 0
Then divide 3 by 2 = 1 + 1
Then divide 1 by 2 = 0 + 1

Read Up

Listing the remainders from *bottom* to *top*, left to right we have 11001; the binary form of $(25)_{10}$ is $(11001)_2$.

Conversion of the decimal system to any number system requires only division by the base of that number system, keeping track of the remainders, and reading the answer from the last remainder to the first.

Now we can change numbers back and forth at will. But what about fractional numbers? They aren't too bad if we remember that negative powers work in much the same way as positive powers. Let's go back to the general equation for base 10 and use negative exponents.

$$N = d_1 \times R^{-1} + d_2 \times R^{-2} + d_3 \times R^{-3} + \ldots + d_n \times R^{-n}$$

For binary, we have

$$N = d_1 \times 2^{-1} + d_2 \times 2^{-2} + d_3 \times 2^{-3}$$

Then, if we pick a fractional number 0.621, we can write the decimal form

$$0.621 = 6 \times 10^{-1} + 2 \times 10^{-2} + 1 \times 10^{-3}$$

$$0.621 = 0.6 + 0.02 + 0.001$$

$$0.621 = 0.621$$

Similarly, a fractional binary number $(0.1001)_2$ may be written as

$$(0.1001)_2 = 1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$$

or

$$(0.1001)_2 = 1 \times \frac{1}{2^1} + 0 \times \frac{1}{2^2} + 0 \times \frac{1}{2^3} + 1 \times \frac{1}{2^4}$$

$$(0.1001)_2 = 1 \times \frac{1}{2} + 0 \times \frac{1}{4} + 0 \times \frac{1}{8} + 1 \times \frac{1}{16}$$

$$(0.1001)_2 = 0.5 + 0 + 0 + 0.0625$$

$$(0.1001)_2 = (0.5625)_{10}$$

Converting fractional binary numbers to decimal numbers is an easy process.

Here is a method that can be used to convert decimal to binary. Suppose the decimal number 0.56531 is to be converted to binary.

First, multiply $0.56531 \times 2 =$ 1.13062
Then multiply $0.13062 \times 2 =$ 0.26124
Then multiply $0.26124 \times 2 =$ 0.52248
Then multiply $0.52248 \times 2 =$ 1.04496
Then multiply $0.04496 \times 2 =$ 0.8992
Etc.

Read Down

Collecting the whole numbers *from the top down* we read the answer as $(0.10010\ldots)_2$.

This can be checked by the previous method.

$$(0.10010)_2 = 1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$$

$$(0.10010)_2 = 0.5 + 0.0625$$

$$(0.10010)_2 = (0.5625)_{10}$$

This process can be carried out to any number of places required. When the answer is not accurate enough, the process may be carried out to more places until the desired accuracy is achieved.

Now that we are familiar with the Binary Number System and how to get from one system to another, it is time to investigate operations in the binary system. In order to understand the computer, we must learn how it makes computations in this number system.

Binary arithmetic is concerned with the same four basic operations found in decimal arithmetic. These basic operations are addition, subtraction, multiplication, and division. We will do some of these operations with pencil and paper to illustrate how the machine does them automatically.

Binary addition has only four possible combinations. The combinations are:

$$0 + 0 = 0 \quad (1.4)$$

$$1 + 0 = 1 \quad (1.5)$$

$$0 + 1 = 1 \quad (1.6)$$

$$1 + 1 = 10$$

or

$$1 + 1 = 0 + \text{carry } 1 \quad (1.7)$$

Since 1 + 1 would be 2, the binary system requires that it be written in two places as 10. This means that the 1 must be carried to the next higher place for addition. So 1 + 1 = 10. An example might help.

Take the decimal number 13, written 001101 in binary and add the decimal 37, written 100101 in binary.

$$\begin{array}{r} 001101 \\ +\ 100101 \\ \hline 110010 \end{array}$$

110010 is the binary form of 50.
1 + 1 = 10, yields the first digit 0, carry the 1.
1 + 0 + 0 = 1, yields the second digit 1, plus nothing to carry.
1 + 1 = 10, yields the third digit 0, plus 1 to carry.
1 + 1 + 0 = 10, yields the fourth digit 0, plus 1 to carry.
1 + 0 + 0 = 1, yields the fifth digit 1, plus nothing to carry.
0 + 1 = 1, yields the sixth digit 1, plus nothing to carry.
Putting all the digits together, we get 110010.

Binary subtraction is the same operation as in decimal. The only tricky thing is zero minus one, which requires borrowing from the next higher position.

We can see that:

$$0 - 0 = 0 \qquad (1.8)$$

$$1 - 1 = 0 \qquad (1.9)$$

$$1 - 0 = 1 \qquad (1.10)$$

But

$$0 - 1 = 1 + \text{borrow} \qquad (1.11)$$

(Because the two of the binary system is in action again, and after borrowing, 2 -1 = 1).

$$\begin{array}{r} 10 = (2)_{10} \\ -\ 01 = (1)_{10} \\ \hline 01 = (1)_{10} \end{array}$$

One cannot be subtracted from zero so a one must be borrowed from the next digit, making the binary 10 or $(2)_{10}$. Subtracting a binary one from a binary two leaves a binary one, just as in the decimal system. To check this, add binary 1 + 1 = 0 + carry or 10 or $(2)_{10}$.

Let's try another example:

$$\begin{array}{r} 11011001 \\ -\ 10101011 \\ \hline 00101110 \end{array}$$

The binary 11011001 corresponds to $(217)_{10}$ minus 10101011, or $(171)_{10}$ equals 00101110 or $(46)_{10}$. These numbers can be verified by the technique described earlier.

There are some other methods for binary subtraction but they will not be discussed here.

The next operation to be discussed is that of binary multiplication. It is a quite simple operation. Actually, the computer performs multiplication by repeated addition. In order to examine how the system works, let's consider the following example:

$$\begin{array}{r} 110101 \\ \times\ \ 111 \\ \hline 110101 \\ 110101 \\ 110101 \\ \hline 101110011 \end{array}$$

or $(53)_{10} \times (7)_{10} = (371)_{10}$.

There is an easy way to add. It consists of a few simple rules.

1. Count the number of ones + carries.
   A. If the resulting number is even, the sum is zero.
   B. If the resulting number is odd, the sum is one.
2. Count the pairs of ones to determine how many ones are to be carried to the next higher position. Be sure to count the carried ones in the pairs.

Binary division is as simple as binary multiplication. Quotients other than one or zero are impossible.

$$
\begin{array}{r}
1100 \\
110\overline{)1001000} \\
110 \\
\hline
00110 \\
110 \\
\hline
00000
\end{array}
$$

By using your conversion, you will find that binary 110 = $(6)_{10}$, $(1001000)_2 = (72)_{10}$, and $(1100)_2 = (12)_{10}$. It is easy to see that if the divisor will not go into the dividend, the divisor cannot be subtracted from the dividend and leave a positive difference.

MATERIALS

Pencil and paper

PROCEDURE

1. Develop the positive integers of the Binary Number System through 100 and record them in figure 1-3A.
2. Convert the following binary numbers to their decimal equivalents and record them in figure 1-3B.

   111011101, 11101101, 10110.1101, .11011, .10001
3. Convert the following decimal numbers to binary and check by converting binary back to decimal and record in figure 1-3C.

   353, 557, 632, .725, .5625
4. Add the following groups of binary numbers and convert the answers. Record in figure 1-3D.

   (a) 1011011 + 1011010

   (b) 110111011 + 100111011

   (c) 0000000110110111 + 0000001101101110 + 0011011011100000 + 1101101110000000
5. Subtract the following, convert the answers and record in figure 1-3D.

   (a) 10110 − 01010

   (b) 100110001101 − 010101110010
6. Multiply the following binary number. Convert the multiplier and multiplicand and check your answer. Record in figure 1-3E.

   110110111 × 10111
7. Divide the following binary numbers. Convert the divisor and dividend. Check the answer. Record in figure 1-3E.

   $1001\overline{)1010001}$

ANALYSIS GUIDE. In this exercise you should develop some ideas about how the computer handles these calculations. Explain how a computer can know that the number it is trying to subtract is smaller than the number to be subtracted from? Discuss why it is useful for a computer to use the Binary Number System. Show how a computer would perform a simple multiplication problem.

Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary
1		26		51		76	
2		27		52		77	
3		28		53		78	
4		29		54		79	
5		30		55		80	
6		31		56		81	
7		32		57		82	
8		33		58		83	
9		34		59		84	
10		35		60		85	
11		36		61		86	
12		37		62		87	
13		38		63		88	
14		39		64		89	
15		40		65		90	
16		41		66		91	
17		42		67		92	
18		43		68		93	
19		44		69		94	
20		45		70		95	
21		46		71		96	
22		47		72		97	
23		48		73		98	
24		49		74		99	
25		50		75		100	

(A)

Binary	Decimal
111011101	
11101101	
10110.1101	
.11011	
.10001	

(B)

Decimal	Binary
353	
557	
632	
0.725	
0.5625	

(C)

Fig. 1-3 The Data Tables

Binary	Decimal
4.(a)	
4.(b)	
4.(c)	
5.(a)	
5.(b)	

(D)

Binary	Decimal
6.	
7.	

(E)

Fig. 1-3 The Data Tables (Cont.)

PROBLEMS

1. What is the answer in binary numerals?

$$\begin{array}{r} 1572 \\ -\ 964 \\ \hline \end{array}$$

2. Give the answer in decimal.

$$\begin{array}{r} 001101 \\ +\ 100101 \\ \hline \end{array}$$

3. $110101 \times 111 \div 87 = ?$

INTRODUCTION. When problems of logic are considered, some interesting mathematical forms can be developed for expression. Boolean algebra is one of these mathematical forms. In this experiment we will examine some of the shorthand notations of Boolean algebra and learn a few Boolean theorems.

DISCUSSION. Some of the principles of logic are quite old. Many were first set forth by Aristotle. He said that there existed certain statements that were either true or false and never partly true or false. In 1847, George Boole, an English mathematician, developed a shorthand notation for these statements.

Boolean algebra employs operations with single value functions having two possible discrete states.

For our purposes, Boolean algebra applies to the binary digits of 0 and 1. When applied to a simple switch, the two values can correspond to "open" and "closed". For convention, the open state is usually labelled 0 and the closed state, 1. Boolean algebra is similar to ordinary algebra and arithmetic. The distributive law applies and factoring and expansion are permitted. It is different in that it is a mathematics in which variables have two possible states. A statement is either true or false. The switch is either "open" or "closed," 0 or 1. What better language could be chosen for a discussion of switch circuits? Boolean algebra provides a convenient method of expressing switching arrangements without drawing the circuit. It provides a means of finding a number of circuits that will perform a given switch function.

Only two operations are permitted in logical algebra. They are addition and multiplication. The basic laws for logic addition are

$$0 + 0 = 0 \qquad (2.1)$$

$$0 + 1 = 1 \qquad (2.2)$$

$$1 + 0 = 1 \qquad (2.3)$$

$$1 + 1 = 1 \qquad (2.4)$$

while for logic multiplication, the laws are

$$0 \times 0 = 0 \qquad (2.5)$$

$$1 \times 0 = 0 \qquad (2.6)$$

$$0 \times 1 = 0 \qquad (2.7)$$

$$1 \times 1 = 1 \qquad (2.8)$$

Equation 2.4 may look a little suspicious to you. Remember that it is a *law*; also remember that 1 is the maximum value in the system. What this law really says is that "all" plus "all" still equals "all", just as nothing plus nothing is still nothing.

The words AND and OR can be substituted in the laws of Boolean algebra and this helps in understanding the meanings of the laws. AND can be substituted for the multiplication sign while OR can be substituted for the addition sign. The laws then become

0 or 0 = 0

0 or 1 = 1

1 or 0 = 1

1 or 1 = 1

0 and 0 = 0

1 and 0 = 0

0 and 1 = 0

1 and 1 = 1

This makes the equation 1 + 1 = 1 read "1 or 1 is still 1" while 1 X 1 = 1 reads "1 and 1 are also still one." This is the meaning of these laws which directly relate to AND and OR circuits in computer logic design. It should be noted here that, while the plus sign is almost universally used to denote OR, the X and the dot (·) are both occasionally used for AND.

Functions may be evaluated in the usual way. However, due to their simplicity, all the possible values may be determined. That is, a Boolean function of two variables has only four possible choices. Given two variables, A and B, we can write *all* of the possible combinations:

$$A = 0, B = 0$$

$$A = 0, B = 1$$

$$A = 1, B = 0$$

$$A = 1, B = 1$$

Since this is true, the Boolean function

$$f(A, B) = A + AB \qquad (2.9)$$

can have only four possible solutions. These arise from the possible combinations given previously and may be written as follows:

For the first combination, A = 0, B = 0
The function f (A, B) = A + AB = ?
Substituting f (0, 0) = 0 + (0) (0) = 0

For the combination A = 0, B = 1
f(0, 1) = 0 + (1)(0) = 0

For the combination A = 1, B = 0
f (1, 0) = 1 + (1) (0) = 1

For the combination A = 1, B = 1
f (1, 1) = 1 + (1) (1) = 1

Careful inspection of the answer column for these expressions will reveal that the answer corresponds to the value substituted for A. From this fact, we can observe that:

$$A + AB = A \qquad (2.10)$$

This theorem is called the law of absorption.

The real value of Boolean notation is that it follows the laws of many physical systems. For our purposes, it manifests itself as *switching logic.*

Consider the electrical systems of two switches each, figures 2-1 and 2-2. In figure 2-1 an output is possible only if both A and B are closed. In figure 2-2 an output is available

Fig. 2-1 Two Switches in Series

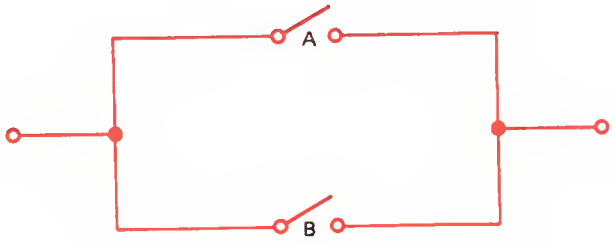


Fig. 2-2 Two Switches in Parallel

SERIES SWITCHES

A	B	Output
Open	Open	No
Closed	Closed	Yes
Open	Closed	No
Closed	Open	No

PARALLEL SWITCHES

A	B	Output
Open	Open	No
Closed	Closed	Yes
Closed	Open	Yes
Open	Closed	Yes

Fig. 2-3 Possible Switch Combinations

if either A or B is closed. The table in figure 2-3 lists all the possible combinations for both sets of switches.

Substituting 0 for open (or on) in the switching tables gives us two tables which correspond to Boolean multiplication and addition. These tables are shown in figure 2-4.

This table illustrates an important fact. Series switches can be used to represent multiplication and parallel switches can be used to represent addition. This is a very important application of Boolean algebra for us, because it can be used to describe switch or transistor logic circuits. Not only can multiplication and addition be represented by switch combinations, but switch combinations can be represented by the multiplication and addition operations. This opens the possibility of developing a machine which can do these mathematical operations electronically using switches or transistors.

The *dual* of an algebraic equation is that equation obtained from the original by interchanging certain pairs of symbols. This becomes important to us in our study of Boolean algebra in that the dual of each law is also a law, and each theorem based on the law has a dual. This saves much time. For example, the law 0 + 0 = 0 has as its dual 1 X 1 = 1, when 1 is substituted for 0 and X is substituted for +. When any theorem in Boolean algebra is proven, its dual is automatically accepted.

Many theorems can be developed for Boolean algebra. When we restrict the pos-

BOOLEAN MULTIPLICATION
(Series Switches)

A	B	AB
0	0	0
1	1	1
0	1	0
1	0	0

BOOLEAN ADDITION
(Parallel Switches)

A	B	A + B
0	0	0
1	1	1
1	0	1
0	1	1

Fig. 2-4 Boolean Multiplication and Addition

sible number of variables to 0 and 1, a method of proof presents itself which is normally impossible in regular algebra because of the infinite number of values which may be assigned to the variables. This method of proof is called the *exhaustion method* and consists of direct substitution of all the possible combinations of 0 and 1. This can be directly related to switch circuits and the theorems can indeed be demonstrated using switch circuits. The use of theorems allows quick reduction of many complex equations to simpler forms, as well as the design of switch circuits which can perform specific switching functions.

THEOREM NUMBER 1

(a) $A + A = A$ (A or A is A) (2.11)
Its dual (b) $A \times A = A$ (A and A are A)

To prove this we can use a *truth table* and list all of the possible combinations.

A	A + A = ?
1	1 + 1 = 1
0	0 + 0 = 0

The dual theorem $A \times A = A$ can be proven similarly, as below, but actually needs no proof since it is a dual of the addition theorem. Therefore, the proofs of the duals will not be shown after this.

A	A × A = ?
1	1 × 1 = 1
0	0 × 0 = 0

THEOREM NUMBER 2 (Identity Law)

(a) $A + 0 = A$ (2.12)
(b) $A \times 1 = A$

A	A + 0 = ?
1	1 + 0 = 1
0	0 + 0 = 0

THEOREM NUMBER 3 (Identity Law)

$A + 1 = 1$ (2.13)
$A \times 0 = 0$

A	A + 1 = ?
1	1 + 1 = 1
0	0 + 1 = 1

THEOREM NUMBER 4 (Commutative and Associative Laws)

(a) $A + B = B + A$ (2.14)
(b) $A \times B = B \times A$

A	B	A + B = ?	B + A = ?
0	0	0 + 0 = 0	0 + 0 = 0
0	1	0 + 1 = 1	1 + 0 = 1
1	0	1 + 0 = 1	0 + 1 = 1
1	1	1 + 1 = 1	1 + 1 = 1

THEOREM NUMBER 5 (Distributive Law)

(a) $(A + B) + C = A + (B + C)$; (2.15)
$A \times (B + C) = A \times B + A \times C$
(b) $(A \times B) \times C = A \times (B \times C)$

ABC	(A + B) + C = ?	A + (B + C) = ?
000	0 + 0 = 0	0 + 0 = 0
100	1 + 0 = 1	1 + 0 = 1
010	1 + 0 = 1	0 + 1 = 1
001	0 + 1 = 1	0 + 1 = 1
110	1 + 0 = 1	1 + 1 = 1
101	1 + 1 = 1	1 + 1 = 1
011	1 + 1 = 1	0 + 1 = 1
111	1 + 1 = 1	1 + 1 = 1

THEOREM NUMBER 6 (DeMorgan's Law)

(a) $(A + B) \times (A + C) = A + (B \times C)$
(b) $(A \times B) + (A \times C) = A \times (B + C)$ (2.16)

The proof is similar to the other theorems. It is interesting to examine the switch network equivalent for theorem six (a). It will

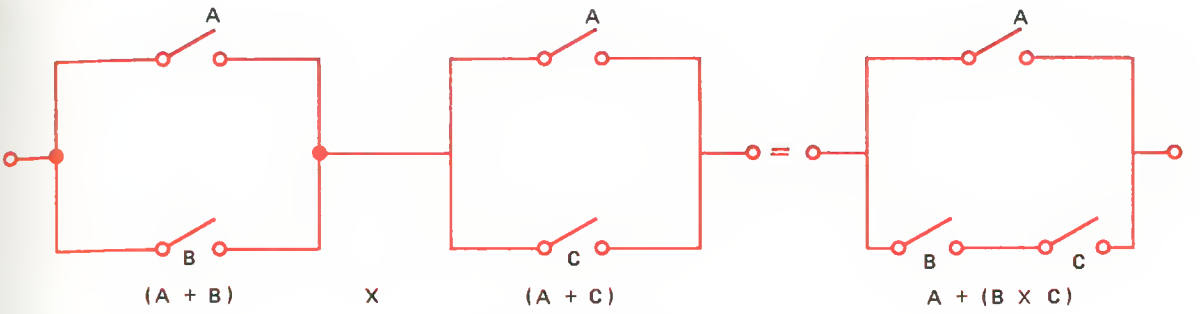


Fig. 2-5 Theorem Six

be found that the two networks are open and closed for the same conditions, and the two networks are equivalent.

THEOREM NUMBER 7 (Absorption Law)

(a) $A + (A \times B) = A$
(b) $A \times (A + B) = A$ **(2.17)**

This theorem may be proven by exhaustion through a truth table. Fig. 2-6 is an electrical representation. This combination shows how difficult networks may be reduced to simple networks

Now we reach a departure from our ordinary algebra. This concept is the "not" function. The not function is usually indicated by the symbol $\overline{A}$ read "A Bar" or the symbol A' read "A Prime." In either case, the symbol indicates "Not A." Zero Bar ($\overline{0}$) indicates "not zero." Since the only other possibility we have in binary is 1, a "not zero" is equal to 1. $\overline{1} = 0$, or "not one" is zero. To continue this to general terms, $\overline{A}$ = Not A. Then, if $\overline{A} = 0$, $A = 1$; or if $\overline{A} = 1$, $A = 0$.

The electrical illustration of this is a *single-pole double-throw* switch. When one set of contacts is "made," the other is "not" made. The following theorems are derived from the "not" function.

THEOREM NUMBER 8 (Double Negation)

$$\overline{\overline{A}} = A \qquad \textbf{(2.18)}$$

Read not (not-A) = A

A	$\overline{\overline{A}}$	$\overline{A}$
0	0	1
1	1	0

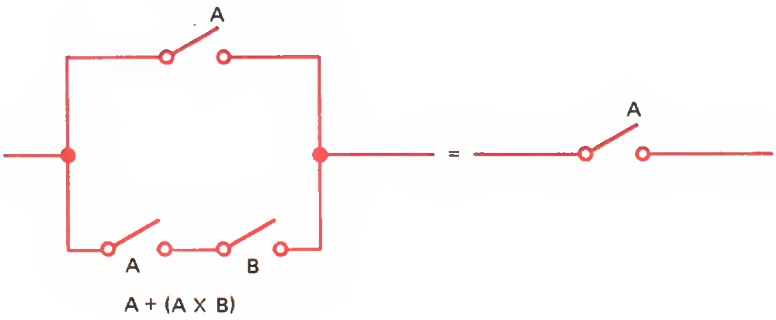


Fig. 2-6 Theorem Seven

Electrically, a switch that was open, but has now been returned to the closed position, illustrates this theorem.

THEOREM NUMBER 9

(a) $A + \bar{A} = 1$ (2.19)
(b) $A \times \bar{A} = 0$

A	$A + \bar{A} = ?$
0	0 + 1 = 1
1	1 + 0 = 1

THEOREM NUMBER 10

(a) $\overline{(A + B + C)} = \bar{A} \cdot \bar{B} \cdot \bar{C}$ (2.20)
(b) $\overline{(A \times B \times C)} = \bar{A} + \bar{B} + \bar{C}$

This theorem holds true for any number of variables. Its proof is similar to the others. You may want to work this one (or the following ones) out for yourself.

THEOREM NUMBER 11

(a) $A \times (\bar{A} + B) = A \times B$ (2.21)
(b) $A + (\bar{A} \times B) = A + B$

THEOREM NUMBER 12

(a) $(A + B) \times (\bar{A} + C) \times (B + C)$ (2.22)
$= (A + B) \times (\bar{A} + C)$

(b) $(A \times B) + (\bar{A} \times C) + (B \times C)$
$= (A \times B) + (\bar{A} \times C)$

Now that we have seen several theorems, it is time to examine their usage. These theorems can be used to expand terms, factor and reduce complex polynomials to simpler forms. When we remember that all Boolean expressions can really be switching combinations, the real worth of the system is realized. It gives us a tool which allows understanding of highly complex switching circuits from the design standpoint, as well as providing the ability to investigate existing switching systems. A simple example of each method may help you understand this useful tool.

Example:

Given: $\overline{AB + \bar{C}} + \bar{A}C + B = ?$

Reduce this expression to a simpler form

$\bar{A}\bar{B} \times (\bar{\bar{C}}) + \bar{A}C + B = ?$
Theorem 10 (a)
$(\bar{A} + \bar{B})\, C + \bar{A}C + B = ?$
Theorem 8 & 10 (b)
$\bar{A}C + \bar{B}C + \bar{A}C + B = ?$
Theorem 6 (b)
$\bar{A}C + (\bar{B}C + B) = ?$
Theorem 1 (a)
$\bar{A}C + C + B = ?$
Theorem 11 (b)
$C + B$ = Answer, Theorem 7 (a)*

*Writing the next to last step $\bar{A} \times C + C + B = ?$ makes it look more like 7 (a).

Given the expression

$$A + B + AC = ?$$

draw the switch diagram.

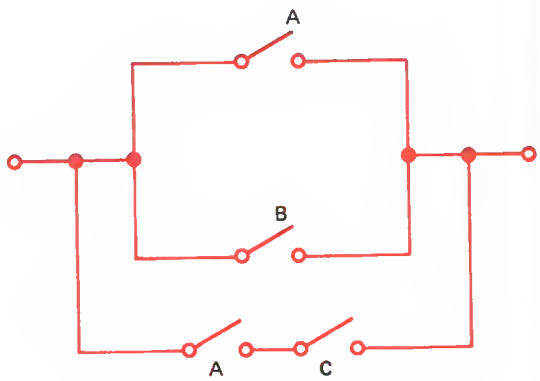


Fig. 2-7 The Example Circuit

Simplify algebraically:

$A + B + AC =$ Rearranging terms by
$A + AC + B =$ Theorem 7 (a)
$A + B =$ Answer

Draw the network.

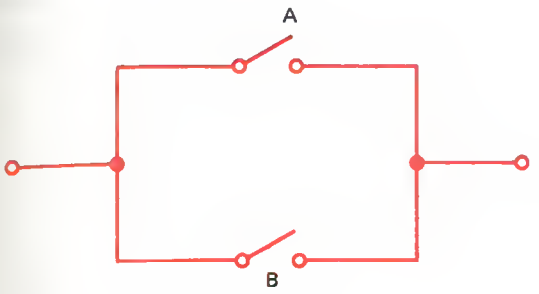


Fig. 2-8 The Simplified Circuit

Many more examples could be given, but these two should be enough to demonstrate the worth of the system. In the highly complex switching circuitry of a digital computer, simplifications of this sort are a great help. With a knowledge of the theorems, we can solve almost any circuit for a workable solution. You should realize that the solution arrived at may not necessarily be the only solution nor even the best. This is because the stage at which we decide to stop the mathematical manipulation is largely a matter of choice. There are no easy rules for manipulating the theorems and expressions. As in algebra, you can start by removing the parentheses (or bars), then study and compare the theorem for application.

Remember, in our field OR (+) represents a parallel circuit while AND (X) represents a series circuit.

Many times in the computer field you will find a set of series switches (electronic, relay, or any other type) referred to as an AND circuit. While a set of parallel switches is referred to as an OR circuit.

MATERIALS

10 SPST switches
3 SPDT switches
1 VOM or FEM

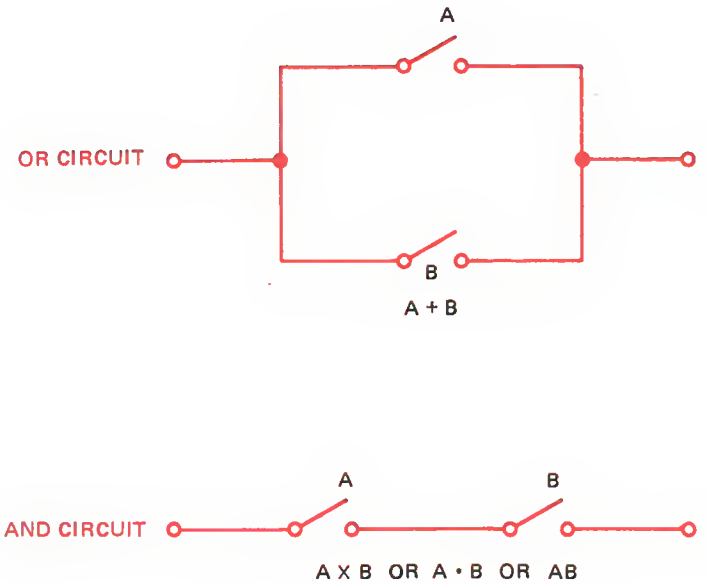


Fig. 2-9 AND — OR Switch Circuits

PROCEDURE

1. Prove theorem 3(b) using the truth table method. SPST switches may be wired to aid you in understanding the theorem. Record the Proof and draw the equivalent circuit.
2. Prove theorem 6(b) and draw the equivalent circuit. Record your results.
3. Construct the experimental circuit in figure 2-10.

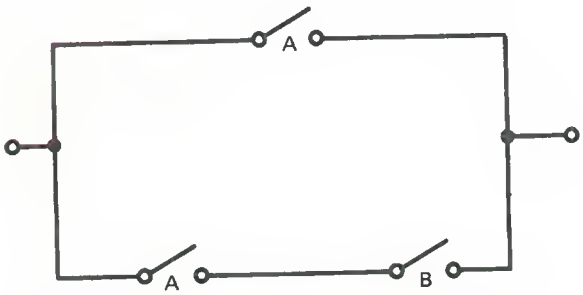


Fig. 2-10 First Experimental Circuit

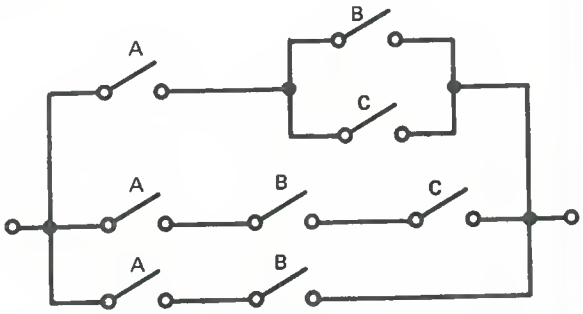


Fig. 2-11 Experimental Switching Circuit

4. Write the Boolean expression for the experimental circuit.
5. Using a truth table, verify the output of the experimental circuit in figure 2-6.
6. Simplify the expression using the theorems and construct the equivalent circuit. Record the steps in the mathematical simplification and draw the simplified circuit.
7. Verify that the simplified circuit produces the same output as the experimental circuit in figure 2-10. Record the truth table.
8. Construct the switch circuit as shown in figure 2-11.
9. Write the Boolean equation for this circuit. Record it in the data table.
10. Develop a truth table for this experimental circuit and record your results.
11. Simplify the circuit as much as you can mathematically and verify your results by the truth table. Draw the simplified circuit.
12. Using single-pole-double-throw switches, construct a circuit and make a truth table for Theorem 8. Record your circuit diagram and truth table results.

ANALYSIS GUIDE. In analyzing the data from this experiment, you should compare the Boolean algebra method of circuit description with the hardwire approach. Do they agree? Which method is easier? Why?

PROBLEMS

1. Simplify $(AB + A) \cdot C$ = output
2. Draw the circuit diagram for the following expression. Do not simplify.

$$wx + wz + wy + x'y'$$

3. Check the identity of each of the following expressions with a truth table.
   (a) $A + A' = 1$ (b) $A \cdot A' = 0$ (c) $(A') = A$

THEOREM 3(b)		A X 0 = 0
	A	A X 0 = 0
	1	X =
	0	X =

THEOREM 6(b)			(A X B) + (A X C) = A X (B + C)
A	B	C	(A X B) + (A X C) = A X (B + C)
			X + X = X + =
			X + X = X + =
			X + X = X + =
			X + X = X + =
			X + X = X + =
			X + X = X + =
			X + X = X + =
			X + X = X + =

TRUTH TABLE FOR Fig. 2-10		BOOLEAN EXPRESSION Fig. 2-10
A	B	
0	0	
0	1	
1	0	
1	1	

Fig. 2-10 SIMPLIFIED EXPRESSION	
A	B

Simplified Circuit

Fig. 2-12 The Data Tables

Fig. 2-11 BOOLEAN EQUATION			
A	B	C	

SIMPLIFIED EQUATION Fig. 2-11			

THEOREM 8	
BOOLEAN EXPRESSION	
A	
1	
0	

Fig. 2-12 The Data Tables (Cont.)

experiment 00011 OSCILLOSCOPE WAVEFORM MEASUREMENTS

INTRODUCTION. The most important tool for waveform analysis is the oscilloscope. In this experiment we will set up an oscilloscope and make some measurements of waveform voltage.

DISCUSSION. An oscilloscope is really little more than a special kind of voltmeter. Instead of a meter movement with a pointer, it has a cathode ray tube (CRT) with an electron beam. The deflection elements cause the beam to deflect in much the same way a voltmeter deflects its pointer. The deflection in both cases is proportional to the voltage applied.

Another special feature of the oscilloscope is the fact that the electron beam is able to follow very rapid changes in the applied voltage. By thinking of the oscilloscope spot as the end of the voltmeter pointer, we can visualize the trace as a two-dimensional display of the horizontal and vertical voltages applied to the oscilloscope deflection circuits. In less expensive oscilloscopes these two inputs (horizontal and vertical) are often the only ones available (sometimes the cathode of the CRT is also accessible for intensity modulation of the trace.) The more expensive laboratory models have these plus many other features.

A laboratory-type instrument is often the only suitable tool for any serious wave analysis. Most of these units have DC inputs, calibrated vertical attenuators, horizontal time bases and trigger circuits, to name a few items. Among the things they will measure are: DC voltage, AC amplitude, pulse duration, frequency, period, rise time, phase, and wave shape.

The subject of this laboratory exercise covers the measurement aspects that will be primarily useful in waveform analysis. Since no single exercise can cover all the uses of this highly versatile instrument, we will confine our consideration to the ones most necessary for analyzing a wave shape.

What are the parameters which are important when considering waveforms? AC amplitude and DC level are probably the first considerations but period and frequency are also very important. The shape with regard to the rise time, duration, and polarity can be determined to establish the type of wave. These are only the most obvious considerations but they do provide us with a starting place.

In order to save time and reduce wasted effort, a technician often adopts a more-or-less standard oscilloscope setup procedure. The following is suggested as a general pattern and will require minor modification for special instruments.

1. Turn **power switch** to off.
2. If appropriate, plug in the desired plug-in unit.
3. Set the **intensity, focus, gain** and **sync** controls to their lowest settings.
4. Set the internal **time base (sweep)** generator to its calibrated position.
5. Set the **sweep selector** switch to the off or external position.
6. Set the **horizontal** and **vertical position** controls to their mid-range positions.
7. Check the power line plug to insure that it is properly plugged in.
8. Turn the **power switch** to the on position.

9. Allow approximately one minute warm-up time before making AC measurements and five minutes before making DC measurements.
10. Carefully advance the **intensity** control until the spot appears on the screen. The lowest intensity setting that produces a clearly visible spot should normally be used to avoid damaging the CRT screen.

    In the event that no spot appears with a maximum setting of the **intensity** control, it is probably because the spot has been deflected off the screen. Resetting the **horizontal** and **vertical position** controls should produce the spot. ONCE MORE, the **intensity** should be turned down before repositioning the deflection controls to avoid damaging the screen with the electron beam.
11. Adjust the **focus** control for a sharp, well-defined spot.
12. Turn up the **screen illumination** control and adjust it to the desired brightness.
13. Adjust the positioning controls for proper positioning of the spot. It should be at the left center of the screen.
14. For triggered sweep oscilloscopes, set the **trigger mode** control to the automatic position. Set the **trigger slope** control to the positive position. (Instruments without triggered sweep should be set to internal sweep.)
15. Set the **sweep magnifier** to X1 position and the **horizontal display** selector to normal sweep.
16. Reposition the trace so that it starts at the left edge of the screen graduation.
17. Make any necessary **focus, astigmatism** and **intensity** adjustments to obtain an easily visible line.
18. When using an oscilloscope with a built-in calibrator, the probe should be checked for correct compensation and calibration (including calibration of the vertical amplifiers, which is usually in the plug-in unit).
19. Note the type of probe to be used, X10, X1, X100, etc.
20. Set the **vertical** amp. **attenuator** to the one volt/cm position.
21. Set the square wave **calibrator** for one volt output. (Watch out for the volts, millivolt selector.)
22. Adjust the **sweep** (variable time base) for approximately one cycle for every two cm of horizontal deflection.
23. Position the waveform for convenient viewing. The amplitude of the square wave should be exactly one cm with no overshoot on the waveform leading edges. Figure 3-1 shows the proper wave-form appearance.
24. In the event that overshoot or undershoot (positive or negative sloping waveform tops) occurs, adjustment of the probe compensation may be required. Improper probe compensation is illustrated in figure 3-2.
25. With the probe ungrounded, touching the tip with your finger should produce a variation in the trace amplitude dominated by 60 Hz hum. If the probe is grounded with the controls set as described, a clean horizontal line should appear. It is sometimes convenient to set this line on the zero axis (center-line) of the screen. This gives the waveform a zero reference.

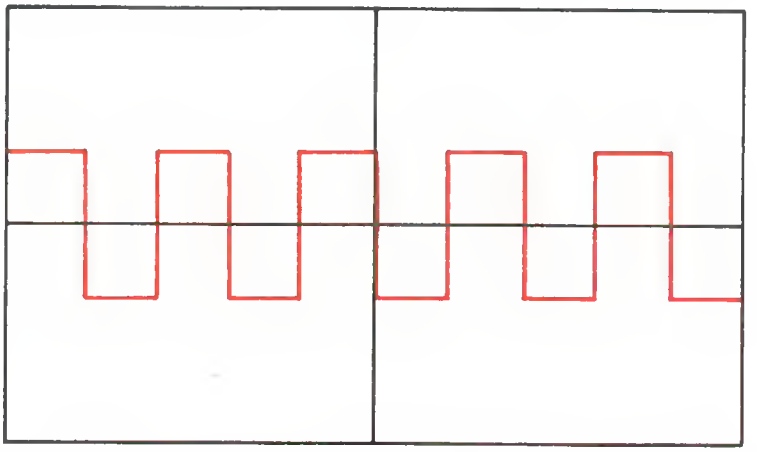


Fig. 3-1 Properly Displayed Square Wave One Volt Calibration — Probe Properly Adjusted

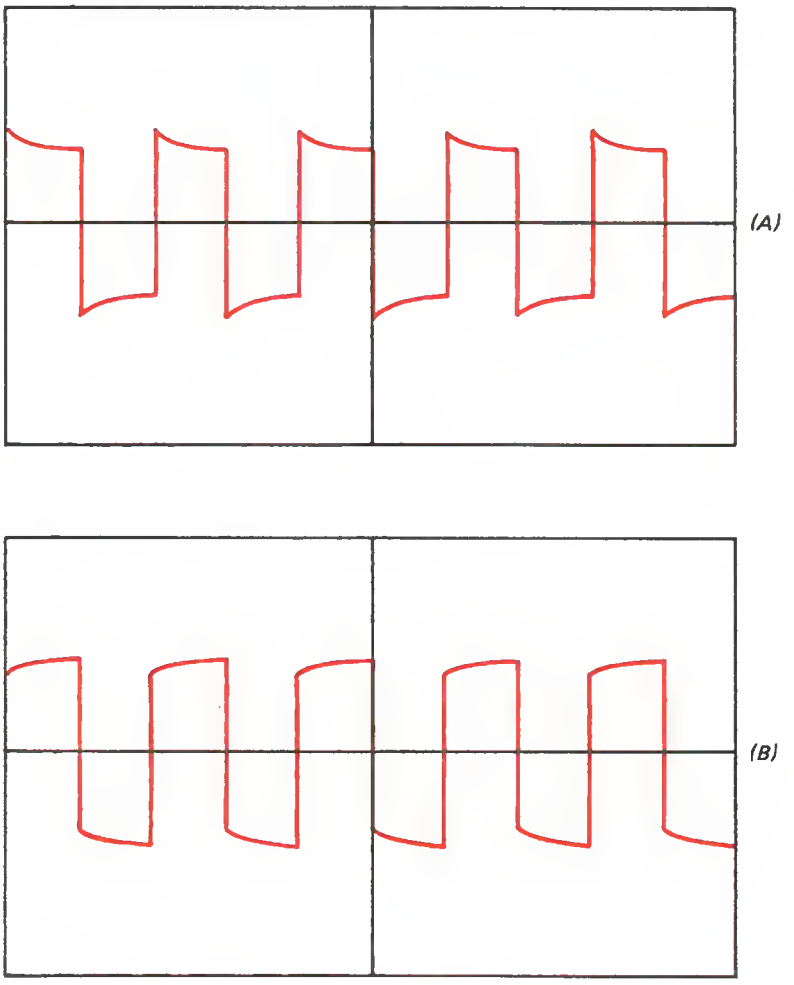


Fig. 3-2 (A) Overcompensated Probe
(B) Undercompensated Probe

The foregoing steps are somewhat lengthy to list and read, but, in fact, take little time to actually perform. They may have to be modified to fit the particular instrument you will be using. You should practice setting up your scope until you can do it quickly without directions.

After the setup steps are completed, the oscilloscope is ready to accept an input signal for measurement. With most instruments the normal signal to be measured is applied to the vertical amplifier. The voltage of the input signal produces a corresponding vertical deflection of the CRT trace. In laboratory instruments the vertical amplifier is provided with calibrated attenuators for precise amplitude measurement (in most cases, voltage measurement). By counting the graduations on the face of the CRT and applying the multiplication factor to the input attenuator (Don't forget the probe attenuation), the voltage of any part of the wave shape can be determined.

Another useful measurement is that of the frequency of the wave. Using a laboratory instrument with a calibrated horizontal time base, the period of any part of the particular wave shape can be found.

All frequency measurements with the oscilloscope are based on time measurements. This is achieved by comparing the incoming wave period to the internal sweep time of the instrument. Some oscilloscopes have a time base generator which is controlled by a front panel knob calibrated in frequency units. In this case the time base is such that the period-to-frequency calibrations are automatic.

In any oscilloscope, if the time period for one complete cycle can be determined, the frequency can be calculated. This is possible since frequency is the reciprocal of the time duration. In pulse or digital work, an instrument with a calibrated sweep control is most desirable. For that reason thisdiscussion will be limited to this type of oscilloscope.

First we will consider how to measure duration. This measurement becomes important in digital work for determining the width and frequency (pulse repetition rate or frequency.) It is convenient to use the following steps in making time measurements.

1. Place the oscilloscope in operation according to your setup procedure.
2. Set the vertical attenuator to a deflection factor which will display the expected signal without overdriving the vertical amplifier.
3. Apply the signal to be measured to the vertical input.
4. Set the sweep trigger slope and mode to Internal, + and Automatic, respectively.
5. Adjust the sweep rate (time/cm) until a convenient number of divisions between the points on the waveform to be measured can be viewed. Due to nonlinearity at the beginning and end of the sweep, it is recommended that the extreme edges of the screen not be used. Normally, the fastest reasonable sweep rate will be best for easy calculations.
6. The horizontal and vertical position controls may be used to position the waveform as needed for measurement.
7. Count the number of centimeters between the points on the waveform to be measured (figure 3-3). Make sure the sweep variable control is in the calibrated position before taking the reading.
8. The time duration between the two points can be determined by equation 3.1.

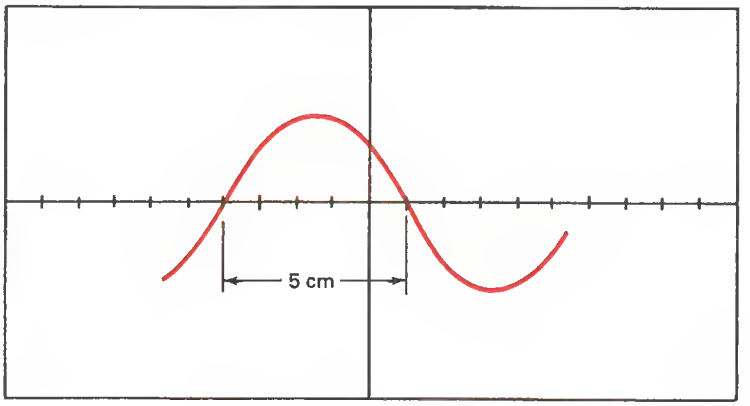


Fig. 3-3 Time Duration

$$\text{Time Duration} = \frac{\text{horizontal distance (cm)} \times \text{horizontal sweep setting}}{\text{magnification}} \qquad (3.1)$$

For example: Horizontal distance = 5 cm (figure 3-3)
Horizontal sweep speed = 0.1 ms/cm
Sweep normal (magnification X 1)

Substituting in 3.1,

$$TD = \frac{5 \times 0.1}{1} = 0.5 \text{ milliseconds}$$

Once the time duration is found, only one more calculation is required to obtain frequency.

$$\text{Frequency} = \frac{1}{\text{Time Duration}} \qquad (3.2)$$

To continue the example,

$$f = \frac{1}{0.5 \text{ ms}} = 2000 \text{ Hz}$$

This procedure covers the major considerations for measuring time duration and frequency. One other major measurement should be considered in order to have a good foundation for pulse and digital work.

This last measurement we wish to consider is that of **rise time.** In theory, square wave and pulses are perfectly square and have instantaneous rise times. In practice, however, a finite amount of time is required for the voltage to rise to the top of the waveform. Simply, then, the rise time could be considered the time required for the voltage to reach its maximum. To eliminate the corners and to give a more constant value, *rise time is defined as the time required for the voltage to rise from 10% to 90% of its total excursion.* Rise time is shown in figure 3-4.

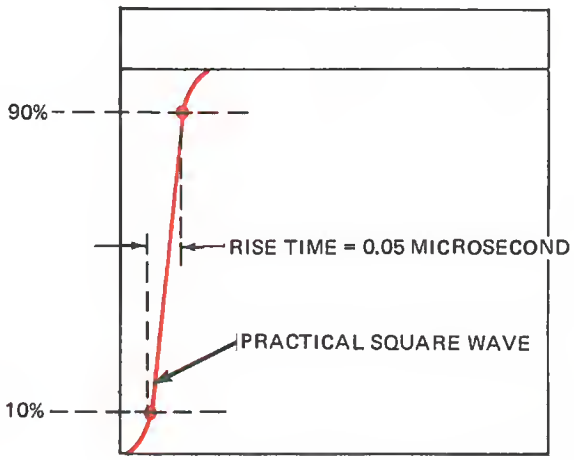


Fig. 3-4 Rise Time

With a good scope that has a calibrated sweep, rise time can be easily measured. It can be read directly from the screen using the method discussed for time duration measurements. The only difference is in the positioning of the waveform so as to be able to read the time duration between the 10% and 90% points.

There are a few points relative to rise time measurements that are worth remembering. The instrument used to measure rise time must have considerably better characteristics than the unit under test. That is, if a scope is being used to check the rise time of a signal generator, the scope must have a much faster rise time than the generator.

As a rough measure, the rise time of an amplifier is about 1/3 of the period at the high frequency cutoff. This says that a scope with a pass band of 4 Hz has a rise time in the vicinity of 0.08 μs. Four megahertz have a period of 0.25 microseconds; therefore, the rise time of a four megahertz scope is about

$$1/3 \times 0.25\ \mu s \text{ or } 0.08 \text{ microseconds}$$

MATERIALS

1 Oscilloscope with probe
1 DC power supply (0-40V)
1 Function generator
1 VOM or FEM

PROCEDURE

1. Set up the scope using the procedure outlined in the discussion.
2. Calibrate the probe using the procedure outlined in the discussion.
3. Set the DC power supply to approximately 10 volts.
4. Measure the DC voltage with the oscilloscope and with the multimeter.
5. Repeat steps three and four for one volt differentials to 15 volts.
6. Apply a IV peak to peak 100 Hz sine wave to the oscilloscope vertical amplifier.
7. Read the amplitude of the signal with the scope and with the multimeter.
8. Repeat steps 6 and 7 in IV steps up to five volts.
9. Apply a 30 Hz sine wave to the scope input.
10. Read and record the time duration of one-half cycle.
11. Repeat steps 9 and 10 for 60, 100, 200, 500, 1000 Hz.
12. Determine the frequency of each wave using your period measurements.
13. Apply a 100 Hz pulse or square wave to the scope.
14. Determine the rise time of the signal.
15. Repeat 13 and 14 for 500 Hz and 1 kHz.

ANALYSIS GUIDE. In analyzing these data you should compare the accuracy obtained using the oscilloscope to that obtained with the multimeter for AC and DC voltage measurement. Discuss the reasoning behind the use of a calibrated horizontal sweep as a basis for measuring period and frequency.

DC Volts	10	11	12	13	14	15
Power Supply Reading (Multimeter)						
Oscilloscope Reading						

Audio Generator Hz	30	60	100	200	500	1000
Time Duration 1/2 Cycle						
Frequency						

AC Volts	1	2	3	4	5
Multimeter Reading					
Oscilloscope Reading					

Frequency	100 Hz	500 Hz	1 kHz
Rise Time			

Fig. 3-5 The Data Tables

PROBLEMS

1. Why is it necessary to have a faster rise time on the scope used to make the measurement than the instrument under test? If this is not so, what does the rise time measured correspond to?
2. What is the period of a 1 kHz waveform?
3. A certain waveform has a horizontal deflection of 8 cm for one complete cycle. The horizontal sweep control is set to 0.1 millisecond/cm. The sweep magnification is off. What is the time duration of the entire cycle? What is the frequency of the waveform?

experiment 00100 BASIC WAVEFORMS

INTRODUCTION. Waveforms are used in logic circuits to transmit information to the individual logic devices. In this experiment some of the basic waveforms will be examined and their characteristics considered.

DISCUSSION. Logic devices are of tremendous importance to us. The complex computers of this age allow us to travel in space as well as to do our ordinary household chores. These devices are usually thought of as being largely electronic, and it is true that electronics plays a major role. However, it is a mistake to believe that all logic is electronic. Logic, like all basic principles, spans the realm of physical science and even enters the area of philosophy and the mind in human encounter. Logic is a tool used by the first and most basic computer, the human mind.

For our purposes we can narrow the application to some specific areas of the physical sciences. These areas are electronics, mechanics, hydraulics and pneumatics. It is true that most of the language (in fact, at the present time, the application of logic) is in the electronic field, but the past few years have seen rapid development in the non-electronic areas of logic as well.

Logic in any physical form deals with the parameters of the field of application corresponding to voltage, current, and power transmission. These parameters are combined to produce waveforms and pulses in the medium used for the passage of information. The medium can be air, oil, water, copper, etc. Because electricity and electronics have been operating in this area, the language, methods, and techniques are well-defined. For this reason we will use electronics as the vehicle for our study, keeping in mind the fact that the principles are applicable to a variety of mediums.

Basic to the study of logic is the study of waveforms. They are used to code or tell the logic circuits what to do by changing the magnitude, shape, frequency, etc., which includes the changing of direction or level of a current or voltage.

Fortunately, highly sophisticated and very useful tools have been developed for the study of electrical waveforms. The most common of these is the cathode ray oscilloscope. This instrument produces a dot of light which, when properly calibrated as to time and amplitude, will produce a representation of a voltage waveform on the screen of its cathode ray tube. Other devices such as the mechanical strip chart recorders are also used, but the basic principle is the same.

In most cases of interest the pattern of changes will repeat itself at a given rate. When this happens the waveform is said to be periodic. From this concept is developed the idea of frequency. Each repetitive combination is defined as a cycle. The number of times it cycles in a given time period (usually one second) is termed the frequency. The units of frequency are cycles per second and are expressed in Hertz. The time taken to produce each cycle is called the period. The units of period are seconds. The relationship

between the frequency and period of a waveform is

$$f = \frac{1}{T} \qquad (4.1)$$

where f = frequency in Hertz
T = the time in seconds for one complete cycle.

This expression will be used over and over in various forms as we examine wave analysis. It is particularly useful when an oscillosocpe is employed for wave analysis. The horizontal scale on most scopes is directly calibrated in time (or frequency) units. The period of the wave can be found by observing the time duration for one complete cycle. Taking the reciprocal of time duration (or period) will yield the frequency.

Periodic waveforms are easily displayed on a laboratory-type oscilloscope. Since the pattern is traced repeatedly, it can be positioned and measured. Normally it is good practice to use a horizontal time base that will display at least two complete cycles. If only one cycle is shown, there is a danger that inaccuracy will develop due to time lost while the electron beam in the scope is returned to its starting point.

Aperiodic waves are not readily displayed on the ordinary laboratory oscilloscope because these waves, by definition, do not occur at a cyclic rate. They must be displayed on some type of recording oscillograph. Some of these waveforms occur only when the circuit is turned on or off or when a dramatic change of state occurs. Variations of this type are called transients. Sometimes we are very interested in these because of the effect they have on circuits and devices. For the present we will be primarily concerned with periodic waveforms.

Sinusoidal variations are found throughout the physical sciences. They produce the familiar wave pattern called "sine waves" which result from graphing the trigonometric sine function. Sinusoidal waves are mentioned here as a starting point only. They are, generally speaking, of little interest in digital circuits. We will be dealing largely with nonsinusoidal waves. These waves are those of voltage or current whose changes are not sine functions.

There are two methods for analysis of nonsinusoidal waves. The first is a mathematical method in which any periodic waveform can be expressed as a combination of a DC component and a number of pure sine waves of different amplitudes, frequency and phase. The time period of the periodic nonsinusoidal wave will be a whole number multiple of the time period of each of its component sine waves. These component sine waves are called harmonics of the given frequency. The sine wave with the lowest frequency is called the fundamental. The ratio of the frequency of a harmonic to the frequency of the fundamental is the number of the harmonic. For instance, if a fundamental frequency of 200 Hz is given, the third harmonic is 600 Hz and the fifth is 1 kHz. The mathematical process by which these component waves are determined is called Fourier Analysis. Notice that the first harmonic is the same as the fundamental (200 Hz). The Fourier system has all of the advantages of a mathematical representation. Equations can be written whose graphical representation produces the amplitude spectra of the waveform.

The general trigonometric equation for a square wave is

$$e = \frac{4}{\pi}\left[\sin \omega t + \frac{1}{3}\sin 3\,\omega t + \frac{1}{5}\sin 5\,\omega t + \ldots + \frac{1}{(2N-1)}\sin (2N-1)\,\omega t\right] \qquad (4.2)$$

where e = voltage amplitude at any time t
N = term number
(2N – 1) = harmonic number which is always odd
ω = angular velocity of the fundamental

Several things can be determined by observing the general equation for a wave. From equation 4.2 we can tell that this square wave contains only odd harmonics (the 1, 3, 5, etc.). Also there is no DC component because this equation is symmetrical about the horizontal axis (the average value for e, the amplitude, is zero).

Observe the following equation for a sawtooth wave:

$$e = \frac{2}{\pi}\left[\sin \omega t - \frac{1}{2}\sin 2\,\omega t + \frac{1}{3}\sin 3\,\omega t + \ldots \frac{(-1)^N}{N}\sin N\,\omega t\right] \qquad (4.3)$$

From equation 4.3 we can determine that all the harmonics are present (odd harmonics have + signs and even harmonics have –). The wave is symmetrical about the horizontal axis.

The general equation for a rectangular pulse waveform is

$$e = \frac{\theta}{\pi} + \frac{2}{\pi}\left(\sin \omega t \cos \omega t + \frac{\sin 2\,\omega t \cos 2\,\omega t}{2} + \frac{\sin 3\,\omega t \cos 3\,\omega t}{3} + \frac{\sin 4\,\omega t \cos 4\,\omega t}{4} + \ldots + \frac{\sin N\,\omega t \cos N\,\omega t}{N}\right) \qquad (4.4)$$

where $\theta = (\pi)$ (duty cycle)

All harmonics are present and a DC component is present because none of the waveforms fall below the horizontal axis. The duty cycle is the percentage of time the overall wave is at its maximum value.

All of these equations theoretically have infinitely many terms but in application, no more than 10 to 20 sine waves are required to describe a waveform. The higher-numbered harmonics become small enough to be negligible after that. Pulse waveforms may require more harmonics to be adequately represented, depending on the duty cycle. That is, the number of harmonics required is inversely proportional to the duty cycle. This rule is important for short duty cycles only.

After the sine wave, which is normally covered in AC circuit courses, the most prominent basic waveform is the square wave. Let's continue our discussion of square waves using a second method of analysis. In this second method the wave is considered as variations made up of small segments. The segments themselves can be thought of as being one of four basic shapes. These shapes are the sine, step, ramp, and exponential waveforms. A truly square wave is made up of a series of step voltages. A step voltage is a sudden change from one constant voltage

level to another. Theoretically, we like to think of this change as instantaneous. Any change does, however, require some finite length of time. This length of time is usually very short compared with the time of the preceding constant level. This sudden change can be in either the positive or negative direction from the constant level. The amplitude of the step is defined as the difference of the two constant levels. Figure 4-1 shows a square waveform.

The period of the square wave is the time T in figure 4-1. A square wave has a stepped voltage (at a constant level) for a time duration which is equal to one-half the period. This brings up the idea of a rectangular pulse waveform. A rectangular pulse waveform is similar to a square wave in that it is also made up of step function segments. The only practical difference is in the relationship of the time duration to the period. If the square waveform is considered to be made up of square pulses which have an "on" time (when the step function suddenly moves to maximum amplitude) that is equal to the "off" time (step function drops to zero), the square wave is a special case of the general rectangular pulse waveform. The duty cycle of any rectangular

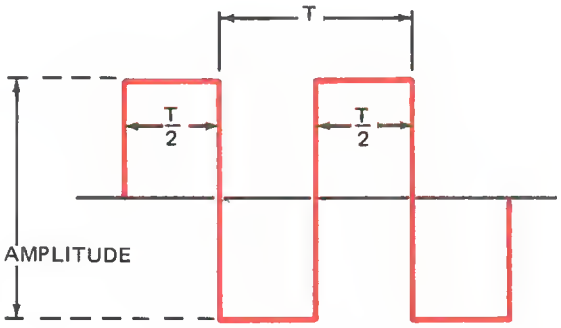


Fig. 4-1 Square Waveform

pulse waveform can be calculated by

$$\text{Duty Cycle (\%)} = \frac{\text{Pulse "on" time}}{\text{Pulse period}} \times 100 \quad (4.4)$$

The square wave can be described as a special type of rectangular pulse having a 50% duty cycle. When the duty cycle falls below the 50% ratio, the waveform is defined as a rectangular wave. A rectangular wave is any wave whose pulse width is less than ten times its pulse duration.

$$\text{Period} < 10\ (\text{pulse duration}) \quad (4.5)$$

This relationship is demonstrated in figure 4-2.

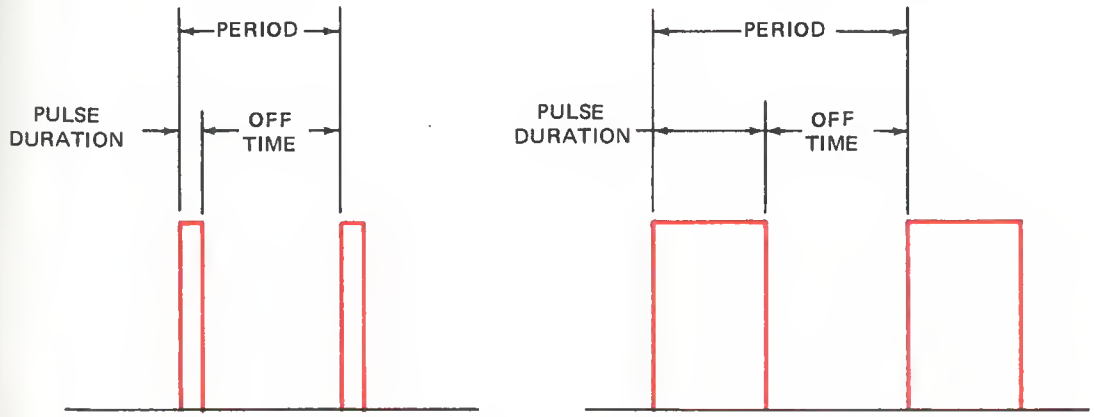


Fig. 4-2 Pulse and Rectangular Waveform

From figure 4-2 it is important to learn that the total pulse period is equal to the pulse duration plus the pulse off time. This can be expressed as

$$T_p = T_d + T_o \qquad (4.6)$$

where T_p = pulse period
T_d = pulse duration
T_o = pulse off time

Pulse waveforms are extremely important to the study of logic. For this reason we will examine them in some detail. We have already noticed the relationship between pulse period and the pulse duration. The duration of a pulse wave shape is much shorter than that of a square wave.

Some terms must be defined that apply to all pulse waveforms including both rectangular and square waves. Referring to figure 4-3, you will notice that the part of the curve labeled leading edge extends from the zero base line to the maximum amplitude. The trailing edge is portion of the curve after the pulse has dwelt through the pulse duration (T_d) and falls to the previous zero or reference level.

Figure 4-3 represents a theoretically perfect pulse waveform. Figure 4-4 represents a more practical pulse. Examination of this pulse reveals that the leading and trailing edges are not instantaneous changes, but require some small amount of time to rise and fall. (These time periods occasionally go by other descriptive names such as build-up time and decay time.) The rise time is that length of time required for the curve to rise from 10% of the average amplitude to 90% of the average amplitude. The fall time is that length of time required for the pulse curve to drop from 90% of the average amplitude to 10%. The average amplitude is the average of the voltage variations during the pulse duration time. Figure 4-4 shows that the top of the pulse is not actually flat, but contains some variations. The rise time and the fall time are not necessarily equal.

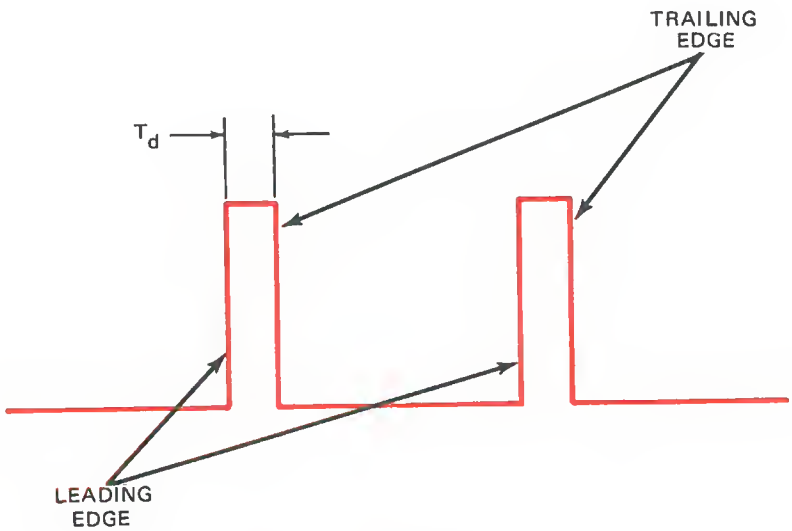


Fig. 4-3 Pulse Waveform

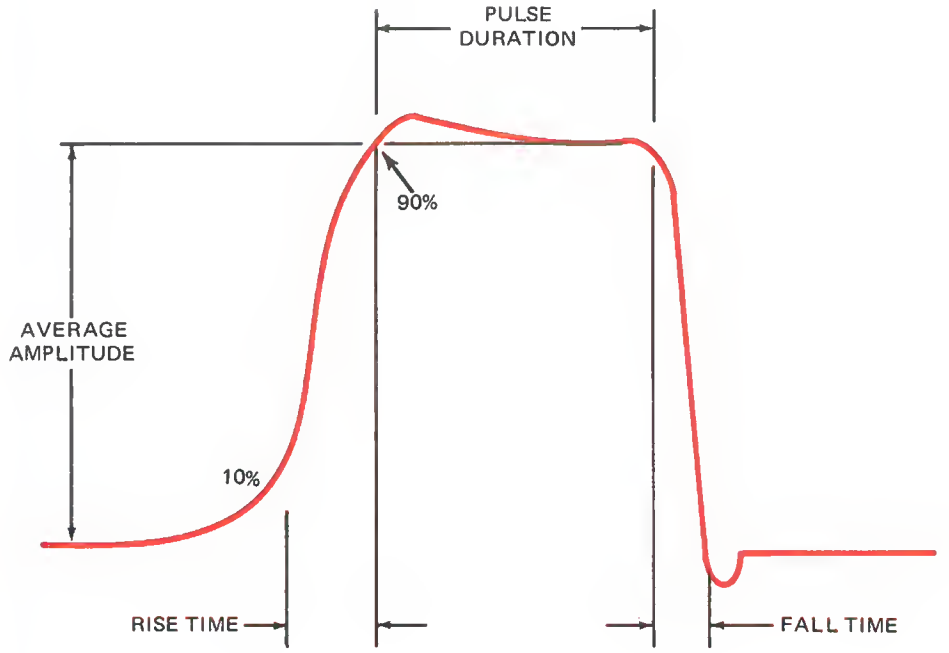


Fig. 4-4 A Practical Pulse

Two other terms are important to the study of pulses. These are the pulse repetition frequency and the pulse repetition rate. The difference between these two terms lies in whether or not the pulses in question are periodic. The term PRF (pulse repetition frequency) is used to designate the occurrence of pulses at a periodic rate within a given time. Pulses that are not periodic are designated by the term PRR. This term gives the average number of pulses during a given length of time. The relationship of the PRF (or PRR) to total pulse period is given in equation 4.6.

$$PRF = \frac{1}{T_p} \qquad (4.6)$$

where PRF = pulse repetition frequency in pulses/sec

T_p = pulse period in seconds

The relationship for the duty cycle is

$$\% \text{ Duty Cycle} = (T_d)\,(PRF)\,(100) \qquad (4.7)$$

This equation can also be written as

$$\% \text{ Duty Cycle} = \frac{\text{Pulse Duration}}{\text{Pulse Period}} \times 100 \qquad (4.8)$$

In cases where the pulse is at least 50 times smaller than the total period, equation 4.8 can be written

$$\% \text{ Duty Cycle} \cong \frac{\text{Pulse on time}}{\text{Pulse off time}} \times 100 \qquad (4.9)$$

This equation is especially handy when using the oscilloscope for making measurements.

In approaching the discussion of triangular and sawtooth waveforms, another basic wave shape must be described. This wave shape is the ramp waveform. It is

a straight line that starts at zero (or any positive or negative voltage) and has a slope that is other than horizontal or vertical. It increases or decreases at a constant rate. When a positive ramp is followed by a negative ramp of the same absolute slope and this sequence is repeated at a constant rate, the result is a triangular wave. A triangular wave is shown in figure 4-5.

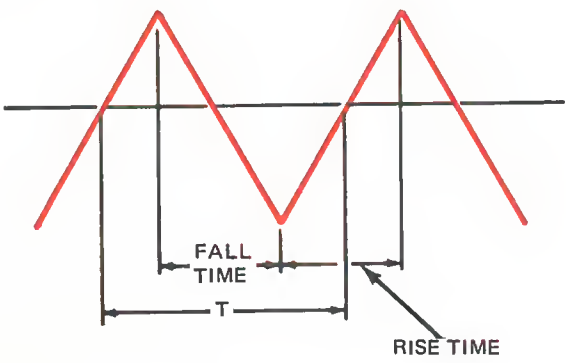


Fig. 4-5 Triangular Wave

The rise time and the fall time of a triangular wave are equal. Triangular waves may be pulse types which do not change direction or alternate in direction with the average value of amplitude for one period equal to zero.

In cases where the slopes and time duration for the positive and negative ramps are not equal while the amplitude remains constant, the resulting wave is a sawtooth. It is usually desirable for the negative ramp (the fall time) to be as short as possible. Thus it actually approaches a step. A finite fall time does, however, occur. Figure 4-6 shows a sawtooth waveform. Practical sawtooth waves often have a rise time that is over 10 times the fall time.

One other wave shape remains to complete our discussion of basic waveforms. This basic waveform is called an exponential waveform. The exponential waveform gets its name from the equation that represents it. An example of an exponential function is the voltage equation

$$e = Ee^{-t/\tau}$$

The graph of this equation is a constantly decreasing curve of negative slope. Exponential waves can result from a resistance-capacitance time constant. The curves can be either positively increasing or negatively de-

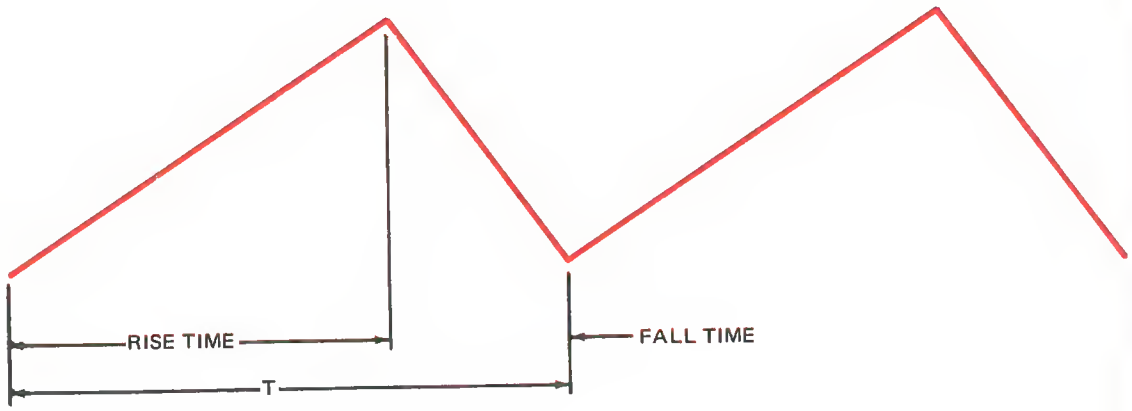


Fig. 4-6 Sawtooth Wave

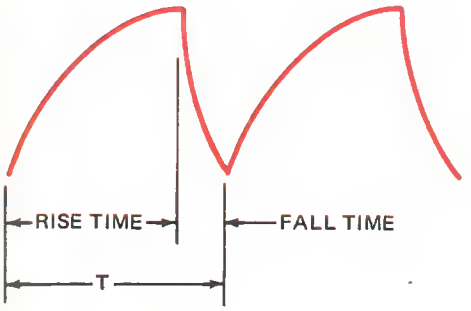


Fig. 4-7 Integrated Square Wave

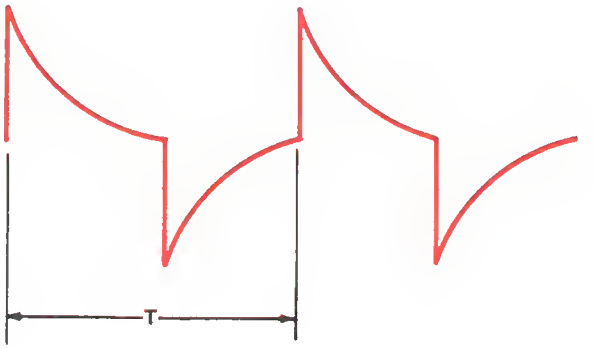


Fig. 4-8 Differentiated Square Wave

creasing exponentials. Figure 4-7 is an example of a wave made up of this type of basic form and is an integrated square wave. This type wave is the result of attenuation of the high frequency harmonics in an amplifier circuit. The reverse of this form occurs when a coupling circuit tends to differentiate the signal. Such a case is shown in figure 4-8.

Many other waveforms appear in many different types of equipment. For the most part these waveforms are made up of different combinations of the four basic waveforms. Some selected examples are shown in figure 4-9. They are trapezoidal and staircase waveforms. Staricase waveforms are used extensively in digital applications for counting.

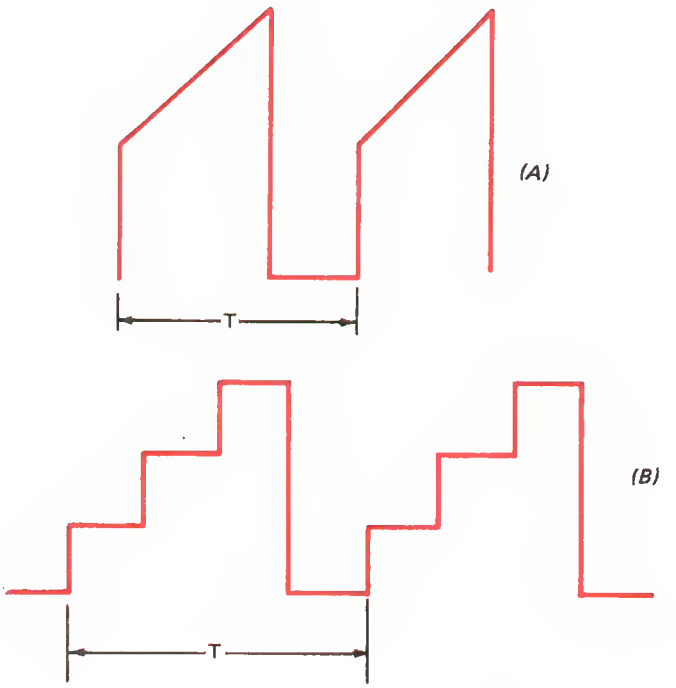


Fig. 4-9 (A) Trapezoidal Wave
(B) Staircase Wave

MATERIALS

1 Oscilloscope
1 Function generator capable of pulse waves
1 0.1 μF capacitor
1 1H inductor

PROCEDURE

1. Set up the oscilloscope for waveform viewing. Be very sure to use a properly calibrated probe.
2. Adjust the function generator to produce a waveform with a 50% duty cycle.
3. Measure and record the time duration.
4. Measure and record the period and frequency.
5. Calculate and record the duty cycle.
6. Measure and record the rise time of the leading edge. (The lab instructor should verify your results.)
7. Measure and record the fall time of the trailing edge.
8. Identify the wave shape and sketch it. (Sketches from the oscilloscope must have horizontal and vertical scales shown.)
9. Place a 0.1 μF capacitor from the output of the signal generator to ground as shown in figure 4-10.

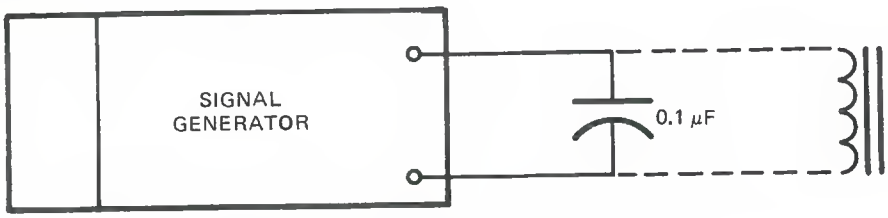


Fig. 4-10 The Experimental Circuit

10. Measure and record the period and frequency.
11. Measure and record the rise time of the leading edge.
12. Measure and record the fall time of the trailing edge.
13. Identify the waveform and sketch its appearance.
14. Replace the 0.1 μF capacitor with a 1H inductor.
15. Measure and record the period and frequency.
16. Identify the waveform and sketch its shape. Then remove the inductor.
17. Set the function generator for 10 kHz pulses with approximately 10 μsec pulse duration. Compare this value as read on the generator dials with that from the scope.

18. Measure and record the PRF. Compare this value with that indicated by the function generator.

19. Sketch the waveform.

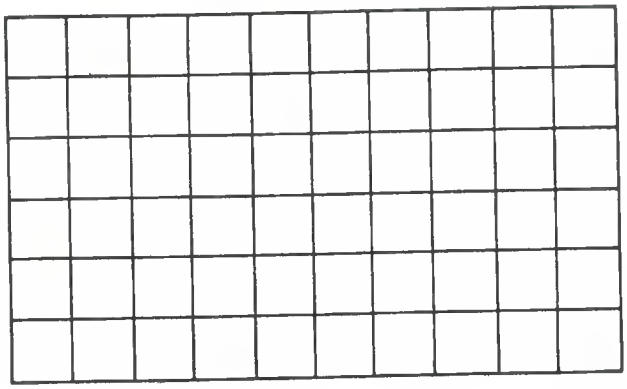
Waveform	Period Set	Freq Set	Period Read	Freq Read	T_d	% DC	T_R	T_F	Identity of Wave
50% DC									
0.1 μF CAP Parallel									
Inductor Parallel									
10 KC Pulse T_d = 10 μsec									

Sketch of First Waveform

Sketch of Second Waveform

Fig. 4-11 The Data Tables

Sketch of Third Waveform



Sketch of Fourth Waveform

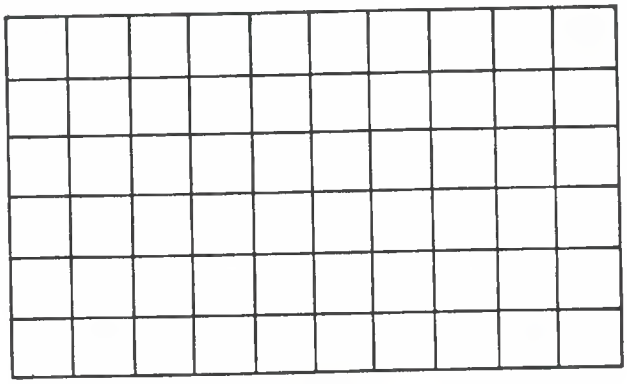


Fig. 4-11 The Data Tables (Cont'd)

ANALYSIS GUIDE. In analyzing these data you should consider the properties of the different waveforms. Consider the effect of capacitance on a waveform and make some comments about the rise time comparisons. Similarly discuss the effect of the inductor on the waveform.

PROBLEMS

1. A certain waveform has a period of 4.14 ms. What is its frequency?
2. What kind of wave contains *only* odd harmonics of the fundamental frequency?
3. A certain pulse has a period of 1 ms and a duration of 0.15 ms. What is its % duty cycle?
4. A narrow pulse has an "on" time of 1.5 μs and an "off" time of 1.0 ms. What is the % duty cycle in this case?

INTRODUCTION. With the development of solid-state electronic devices, high-speed logic circuits have also been developed. In this experiment we will investigate the characteristics of a transistor as a large signal switch for use in electronic logic circuits.

DISCUSSION. Basically, there are two types of bipolar transistors. They are the PNP and NPN types. The schematic of each of these types is shown in figure 5-1. It is easy to tell the types apart if we remember that the emitter arrow always points toward the N material. The three transistor currents are the collector current I_C, the emitter current I_E, and the base current I_B. In a transistor the three currents are related by

$$I_E = I_C + I_B \qquad (5.1)$$

This equation holds for either NPN or PNP type transistors. The direction of the current is reversed from one to the other. That is, assuming electron flow, the I_C and I_B current flows into the PNP device while the I_E current flows out. Figure 5-2 demonstrates these current directions. In the NPN type, I_C and I_B flow out of the transistor while the I_E current flows in. Equation 5.1 is valid for both PNP and NPN transistors but the direction of flow must be appropriate. There are also *leakage currents* which affect the values of I_B and I_C. These currents also affect I_E

Fig. 5-1 PNP and NPN Transistor Symbol

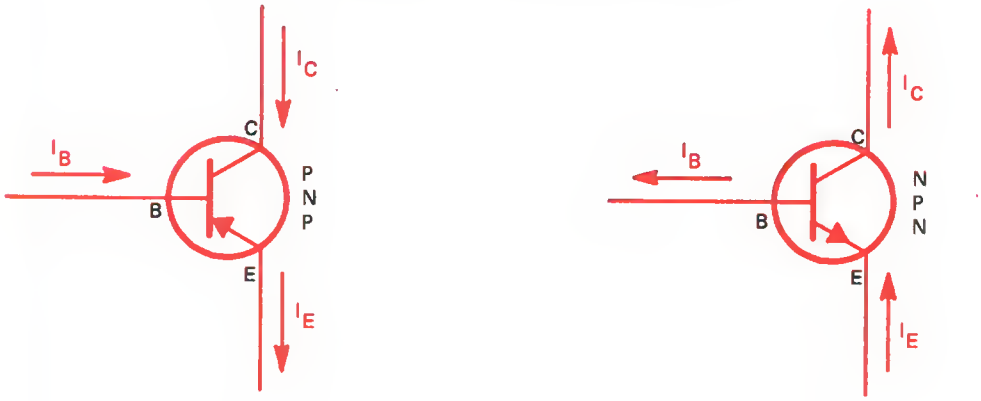


Fig. 5-2 Transistor Current

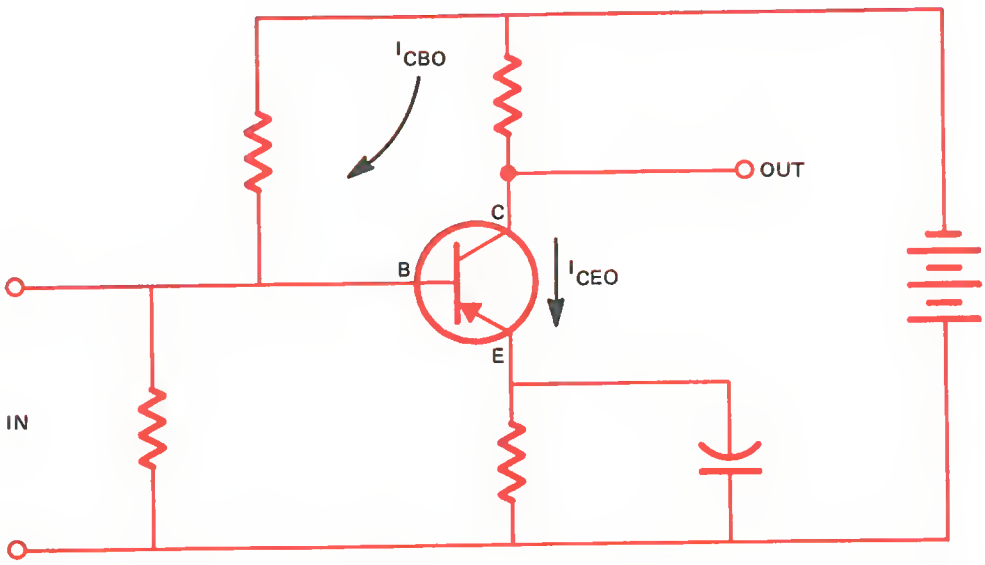


Fig. 5-3 PNP Common Emitter Configuration

because of the relationship given in equation 5.1. Perhaps the most important of these leakage currents is I_{CBO}, the leakage current from collector to base.

The emitter-base junction is normally forward biased as shown in figure 5-3. A reverse bias is applied to the collector-base junction. Under these conditions the I_{CO} (I_{CBO}) that flows must conform to the diode characteristics of this PN junction, as indicated in figure 5-4.

Another leakage current from collector to emitter, called I_{CEO}, can also occur. I_{CEO} is usually larger than I_{CBO} by an amount approximately equal to the current gain of the device. The extra current through the emitter-base junction causes extra heat which tends to increase I_{CO}. If this condition is not controlled, thermal runaway can occur, and the device may be destroyed. Base bias is frequently added to prevent the operating point from changing significantly when I_{CBO} changes.

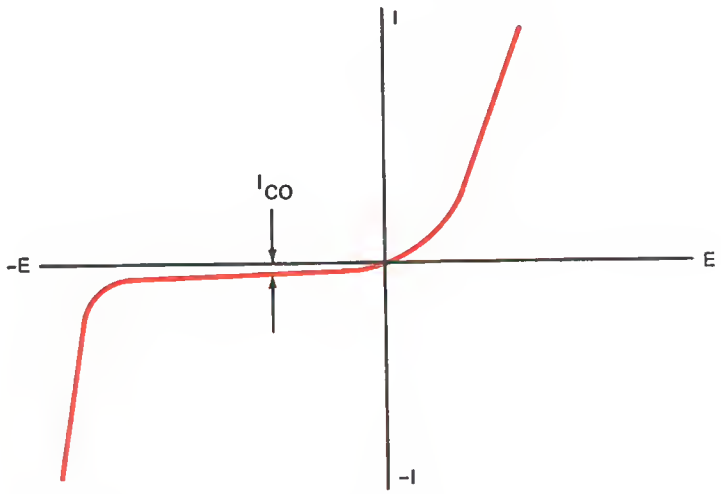


Fig. 5-4 PN Junction Diode Characteristics

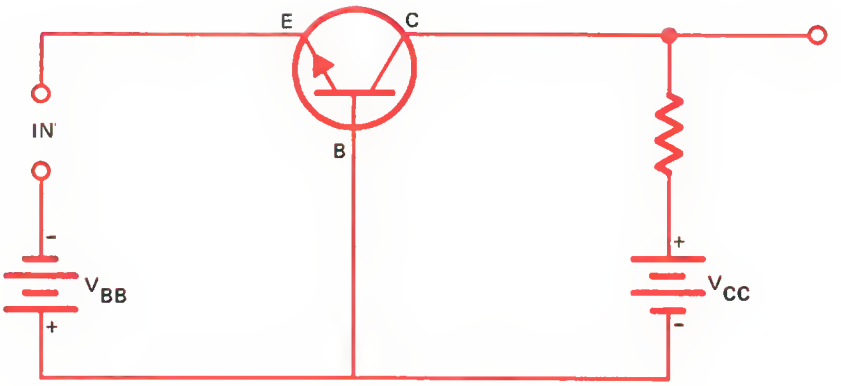


Fig. 5-5 Common Base Configuration

Three different configurations (or connecting methods) are frequently used with either type of transistor. The first of these is the *common-base* connection shown in figure 5-5. The same circuit can be used for a PNP transistor by reversing the battery polarities.

The static current amplification factor can be determined by the expression

$$\alpha_o = \frac{I_C}{I_E + I_{CO}} \qquad (5.2)$$

On the other hand, the dynamic current amplification factor α_{fe} is given by

$$\alpha_{fe} = \frac{\Delta I_C}{\Delta I_E} \qquad (5.3)$$

The value of α_{fe} is usually very near unity.

The common-emitter configuration shown in figure 5-6 is a second frequently-encountered arrangement.

For static conditions, the current amplification factor (β_o) is determined by dividing the collector current by the base current.

$$\beta_o = \frac{I_C}{I_B} \qquad (5.4)$$

For the dynamic condition,

$$\beta_{fe} = \frac{\Delta I_C}{\Delta I_B} \qquad (5.5)$$

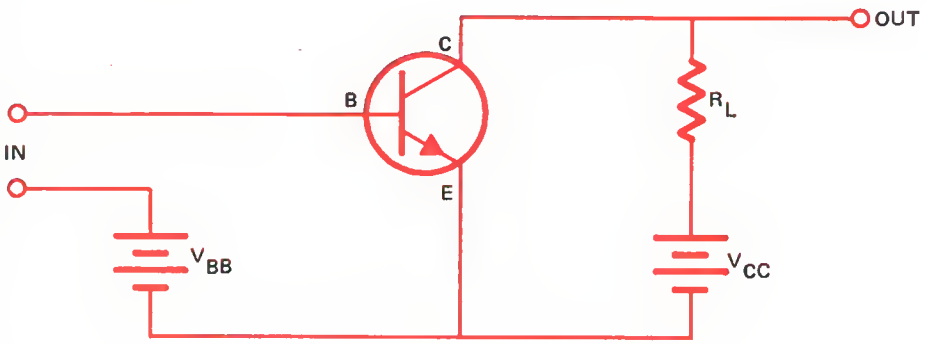


Fig. 5-6 Grounded Emitter Configuration

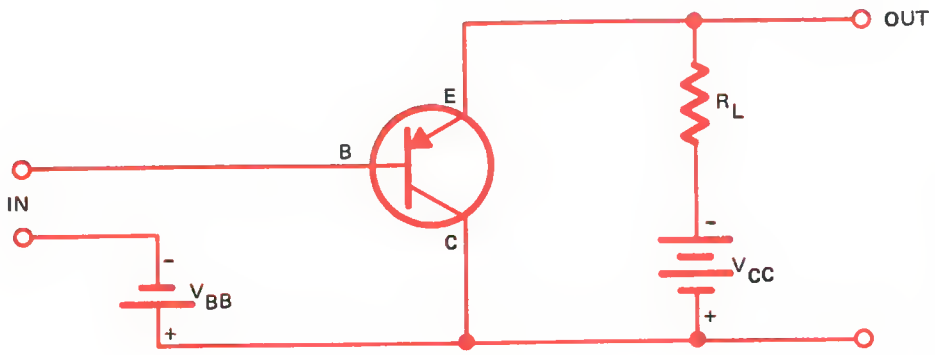


Fig. 5-7 The Common Collector Configuration

A handy relationship exists between α_{fe} and β_{fe}. This relationship is

$$\beta_{fe} = \frac{\alpha_{fe}}{1 - \alpha_{fe}} \qquad (5.6)$$

The current gain, β, is usually higher, having a value of 20 to 200, which causes the power gain to be relatively high (the highest of the three, CB, CE, CC).

The third configuration is the common collector arrangement. The current amplification factor can be determined by

$$A_i = \beta_{fe} + 1 = \frac{\Delta I_E}{\Delta I_B} \qquad (5.7)$$

Notice that the current amplification factor for the common collector configuration is $\beta_{fe} + 1$, or one more than the amplification factor of a common emitter circuit. This allows the common collector configuration to have a higher current gain than a corresponding common emitter circuit. And since $\alpha_{fe} < \beta_{fe}$, the common collector configuration has the highest current gain of the three configurations. At the same time, this configuration has the lowest voltage gain because of its low resistance gain and relatively lower power gain. Its voltage gain is usually approximately equal to one.

Characteristic curves can be determined for each of the three basic transistor configurations. The curves for the common-base and common-emitter are the most useful. The CB input characteristic is a plot of V_{EB} versus I_E with I_C fixed. The value of the input characteristics curve is in finding V_{EB} when I_E is known, or in finding I_E when V_{EB} is known. In both cases, these values correspond to constant values of V_{CB}. The method used is shown in figure 5-8. The known value is projected perpendicularly from its axis to the curve and then from the curve to the axis of the unknown. (Points A and X give a value for V_{EB} when I_E is known. Points B and X' give a value for I_E when a V_{EB} value is given.)

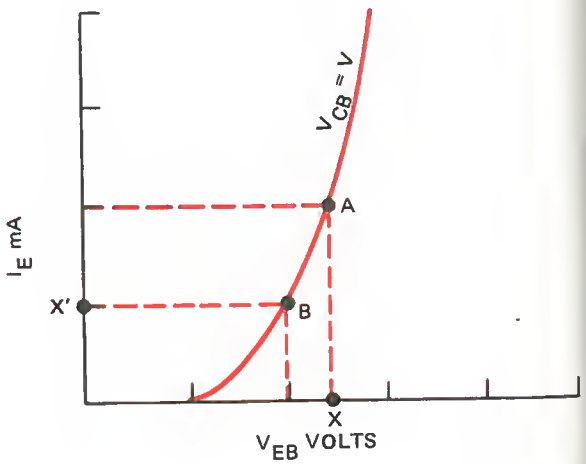


Fig. 5-8 Input Characteristic Curve for CB

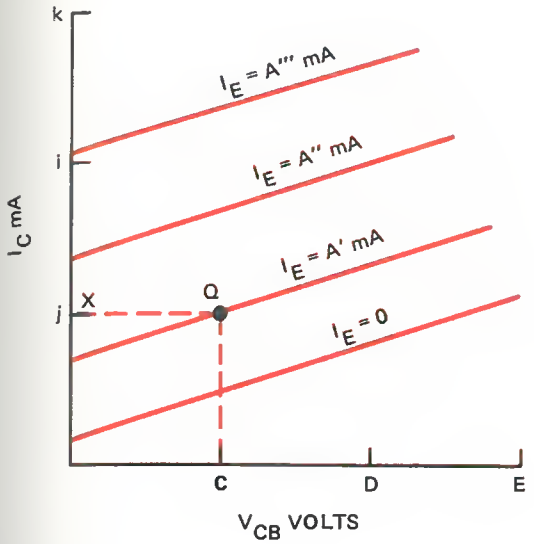


Fig. 5-9 CB Output Characteristics

The output characteristics of a common base circuit are shown in figure 5-9. This curve is plotted with V_{CB} versus I_C for fixed values of I_E. Using these curves (which usually appear as a family), when two elements are known, the third can be found. For instance, if V_{CB} is given as C volts and I_E is given as A' mA, then projecting a line perpendicular to the V_{CB} axis out to the I_E = A' mA line locates point Q. Projecting perpendicularly from point Q to the I_C axis locates point X. The reverse procedure would identify either of the other values.

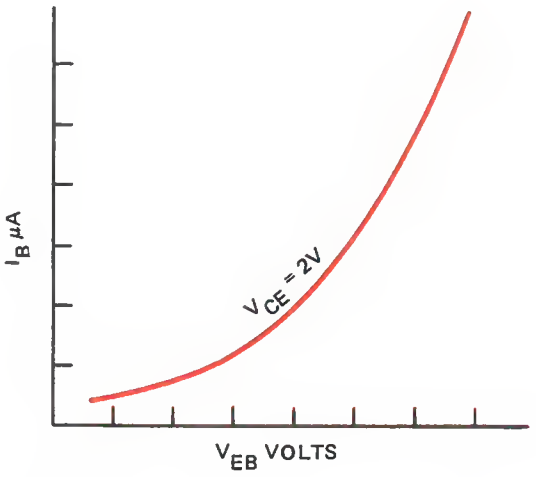


Fig. 5-10 Input Characteristics of CE

Figure 5-10 shows the input characteristic curve for a CE circuit. This is not the only curve that can be drawn to show the input characteristics, but it is one of the most useful.

Figure 5-11 shows the curve that would normally be obtained with a transistor curve tracer. In this family, the I_B curves are parallel,

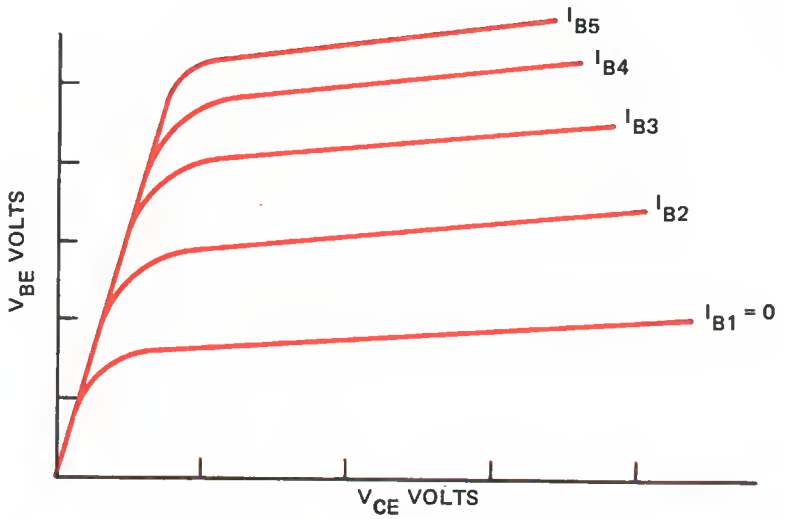


Fig. 5-11 Curve Tracer Input Characteristics of CE

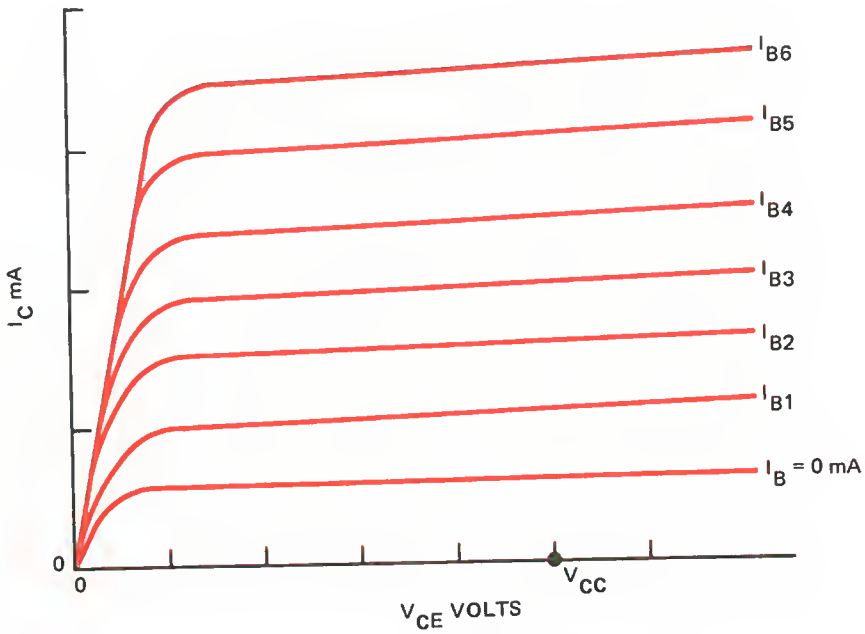


Fig. 5-12 Output Characteristics of CE

tend slightly upward, and become closer at the top. This family is similar to the family shown in figure 5-12, but the nonlinearity has been omitted for simplicity.

These characteristic curves are very important in the design of logic switching circuits. The DC load line is constructed in the normal manner. If certain parameters are required, these are used as starting points. For instance, if V_{CC} is predetermined, this becomes the X intercept. When the load resistance is predetermined, the Y intercept can be calculated from

$$I_{C\ max} = \frac{V_{CC}}{R_L}$$

The Y intercept is the value of I_C which satisfies this equation. R_L can be selected by using the assigned (or chosen) value of V_{CC} as the end point for a family of load lines. Figure 5-13 demonstrates this method. When a suitable I_C is chosen, it can be used to calculate the load resistance.

$$R_L = \frac{V_{CC}}{I_{C\ max}}$$

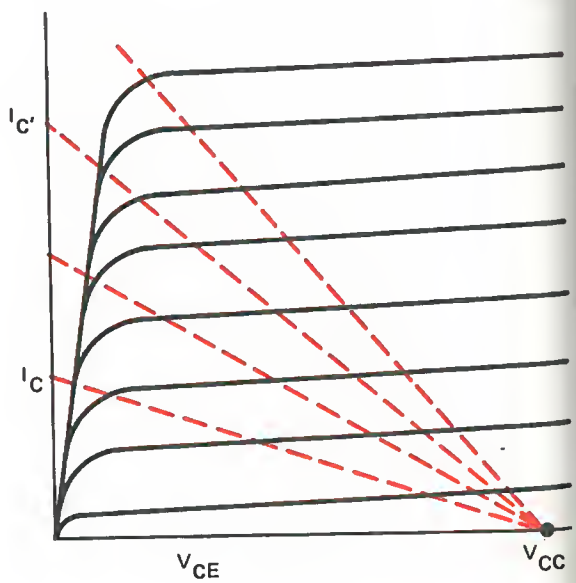


Fig. 5-13 Choosing I_C with the Load Line

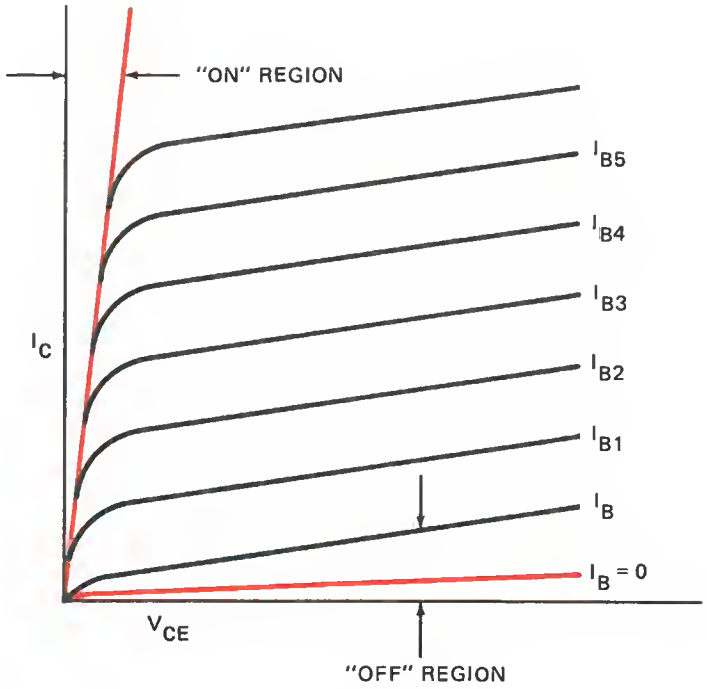


Fig. 5-14 ON and OFF Regions of a Transistor

Load lines for switching transistor applications are not so critical as are those for class A amplifier operation. The transistor spends most of its time in the ON and OFF regions. These regions are shown in figure 5-14. The ON region is often called *saturation,* while the OFF region falls below $I_B = 0$ (no base current flowing, transistor off). This region is past cutoff. The active region contains the area where the curves fall. This is where a class A amplifier would operate. The switching transistor only crosses this region when it is changing from one state to the other. Because it is only operating very briefly in this region, no problem usually develops if our load line crosses the maximum collector dissipation curve.

MATERIALS

2 DC power supplies (0–40V)
2 VOMs or FEMs
1 PNP transistor, type 2N1305 or equivalent
1 Transistor socket
1 1 kΩ, 2W resistor
1 33 kΩ, 1/4W resistor
2 Sheets of linear graph paper

PROCEDURE

1. Connect the circuit shown in figure 5-15. **Be careful about the polarities.**

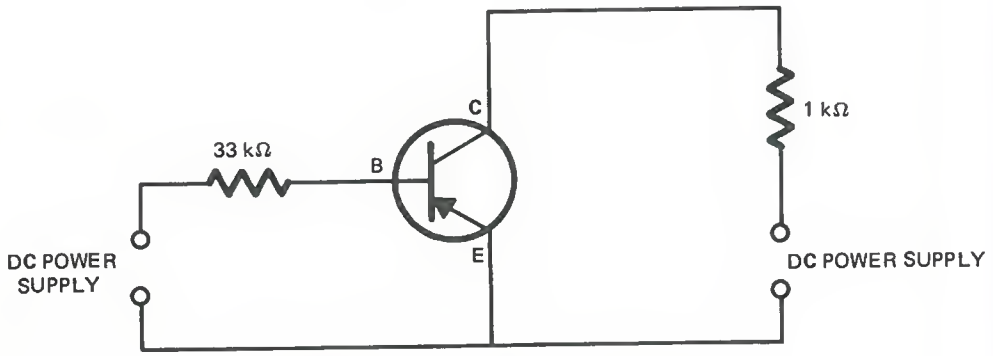


Fig. 5-15 The First Experimental Circuit

2. Set the base current (I_B) to zero.
3. Holding the base current constant, measure and record collector current (I_C) for a series of values of collector-emitter voltages (V_{CE}). Pick 10 to 12 values from zero through 20 volts for V_{CE}.
4. Repeat step 3 holding the base current constant at 40, 60, 80, 100, 120 and 140 μamps. Be certain the base current remains constant during each data run.
5. On a single sheet of graph paper, plot the curves.
6. Disassemble the circuit.
7. Assemble the circuit shown in figure 5-16.

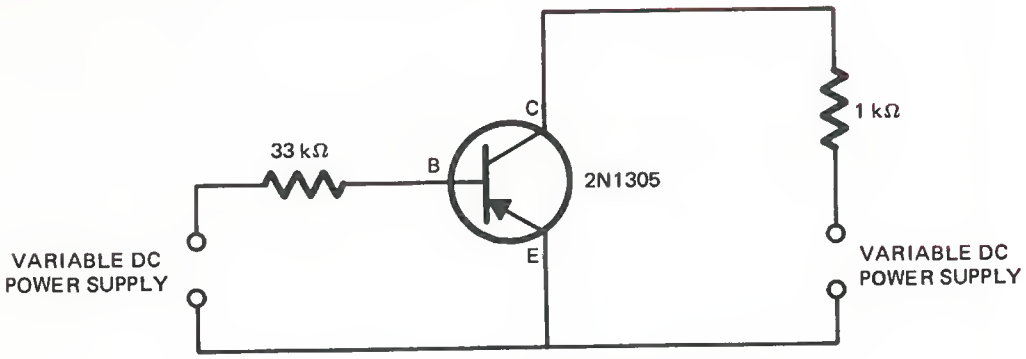


Fig. 5-16 The Second Experimental Circuit

8. Apply -1.0 volt to the collector (V_{CE}).
9. Measure and record the V_{BE} values for I_B = 0, 10, 20, 30, 40, 60, 80, 120, 160 μamps, holding V_{CE} constant at -1.0 volts.
10. Repeat step 8 for V_{CE} values of -5.0, -10.0, -20.0 volts.
11. On a sheet of graph paper, plot the input characteristics of the device.

I_B μA	0	40	60	80	100	120	140
V_{CE} volts	I_C	I_C	I_C	I_C	I_C	I_C	I_C
0							
2							
4							
6							
8							
10							
12							
14							
16							
18							
20							

V_{CE} =	-1.0V	-5.0V	-10.0V	-20.0V
I_B μa	V_{BE}	V_{BE}	V_{BE}	V_{BE}
0				
10				
20				
30				
40				
60				
80				
120				
160				

Fig. 5-17 The Data Tables

ANALYSIS GUIDE. In analyzing these data, careful attention should be paid to the conclusions that can be drawn regarding the transistor characteristics as they apply to switching circuits. The graphs should show the saturation region and cutoff. Did your curves resemble those in the discussion? If yes, how? If no, why?

PROBLEMS

1. Select a suitable V_{CC} and draw a DC load line so that the transistor will operate in the proper region for switching.
2. Calculate the value of R_L in problem 1.
3. Given $V_{CC} = 12V$ and $R_L = 10k$, find I_C using your curves.

experiment 00110 DESIGN OF THE TRANSISTOR SWITCH

INTRODUCTION. Transistor characteristics are the same (more or less) regardless of the application. However, when the device is to be used as a switch, some considerations must be taken into account that are usually disregarded in class A operation. In this experiment we shall examine some of the parameters for a transistor switch.

DISCUSSION. In a class A amplifier the operating point is selected near the center of the active region. Care is taken to choose this point for maximum linearity. This is not an important consideration in switching applications.

In a normal switching circuit, the operating point for the transistor will fall at one extreme of the load line. The upper extreme of I_C is termed the *saturation region,* and the lower limit of I_C is called the *cutoff region.*

Two terms arise dealing with these regions which are used repeatedly in discussions of logic circuits. The first is defined when the operating point of the transistor is in the saturation region. When the device is so operated, the steady-state condition is said to be ON or "normally on." What actually happens physically is that the transistor is conducting as hard as it possibly can under the given conditions. The other possible condition for a transistor switch is OFF. When the transistor is termed OFF, it has an operating point that is in the cutoff region.

To further specify these conditions: OFF means that the device is cut off with no input signal; ON means that the device is normally conducting when no input signal is applied.

In the off condition the transistor should act as much like an open circuit as possible. To achieve this, both the collector-base junction and the emitter-base junction are reverse biased. I_{CO} is the collector leakage current. It flows across the collector-base junction and must be canceled by a reverse bias $I_{B\ OFF}$, which is equal to the I_{CO}.

When operating in its ON condition, the transistor must approach a short circuit as nearly as possible. We do not want the operating point to fall just at the edge of the saturation region, but rather well into the region. For this reason, $I_{B\ ON}$ may be increased beyond minimum saturation to provide reliable switching.

The point of the foregoing discussion is that a reliable and efficient switch must be a high resistance when it is open and a very low resistance when closed. This is true whether the switch is a tube, transistor, or even a mechanical contacter. The ratio of the ON to OFF resistance is important to any switch application and is very important when evaluating transistors to be used as switches. It is practical to expect switching transistors to have ON resistances of under 100Ω and OFF resistances higher than 10 million ohms. The two resistance values can be determined by

$$R_{ON} = \frac{V_{CE\ ON}}{I_{C\ ON}} \qquad (6.1)$$

$$R_{OFF} = \frac{V_{CE\ OFF}}{I_{C\ OFF}} \qquad (6.2)$$

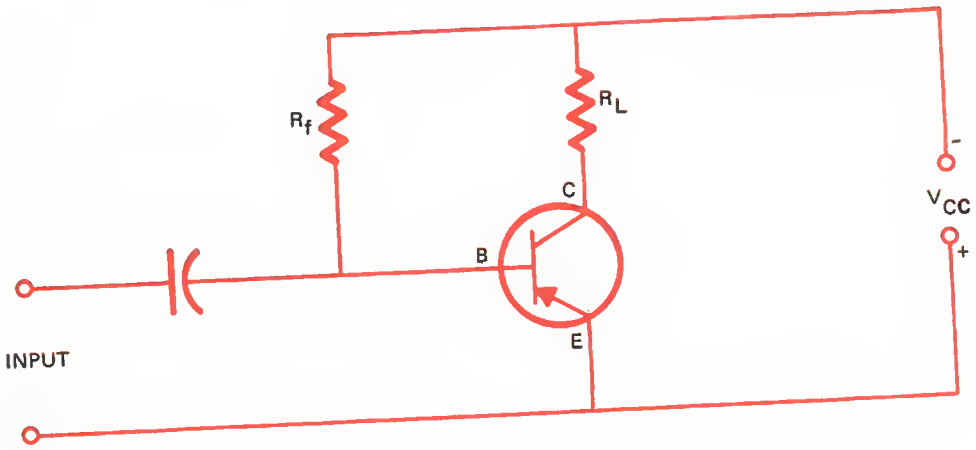


Fig. 6-1 Fixed Bias Transistor Circuit

The ON resistance is the Ohm's Law value determined by the coordinates of the point where the load line crosses the saturation boundary. The OFF resistance corresponds to the coordinates of the point where $I_B = 0$ and the load line intersect. This is the boundary of the cutoff region.

In order to operate the transistor as a switch, we must learn to bias it appropriately. Figure 6-1 shows a circuit for a fixed bias transistor switch. The fixed bias circuit is the simplest and often the least effective. It is actually very seldom used. Its main fault is that it does not compensate for changes in the transistor parameters which will cause a corresponding shift in the operating point. These changes are due to many things including shifts in ambient temperature. Fixed bias is easy to demonstrate and easy to calculate. For these reasons, it is a good starting point for our discussion. The value of the fixed bias resistor is

$$R_f = \frac{V_{CC} - V_{BE}}{I_B} \qquad (6.3)$$

In this case V_{BE} and I_B are the values of the zero signal base operating point.

The problem of holding the operating point fixed is somewhat overcome by applying some self-bias, as illustrated in figure 6-2.

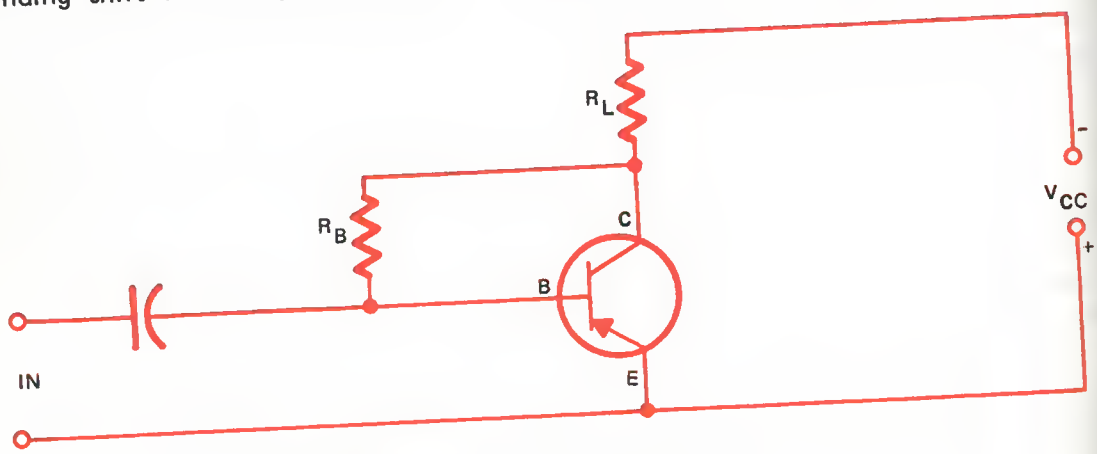


Fig. 6-2 Self Biased Transistor Cirucit

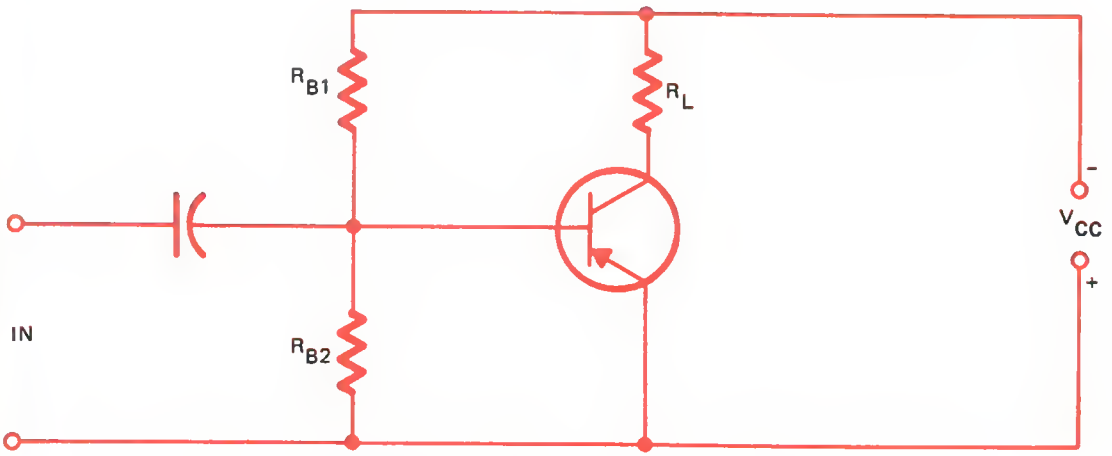


Fig. 6-3 Voltage Divider Bias Transistor Circuit Of Stabilized Bias

R_B supplies a varying bias to provide some Q-point stability. The value of the bias resistor R_B can be found using the values as the ordinates of the zero signal operating point.

The voltage divider bias method provides even more Q-point stability. This method is shown in figure 6-3 and is sometimes called stabilized bias. "Voltage divider" is probably an unfortunate name for this arrangement. In transistor applications, we usually are concerned with current bias. Actually, this situation is no different. The base-emitter bias resistor R_{B2} is chosen by

$$R_{B2} = \frac{V_{BE}}{I_x} \qquad (6.5)$$

V_{BE} is the base-emitter voltage at the zero signal point, and I_x is a value chosen to be equal to or larger than the base current at the zero signal point.

$$R_{B1} = \frac{V_{CE} - V_{RB2}}{I_z} \qquad (6.6)$$

Equation 6.6 is used to choose the other base resistor R_{B1}, where the voltage drop across R_{B2} is subtracted from the collector supply and divided by a current I_z equal to the sum of I_x and the base current of the operating point with zero signal. This system overcomes the inadequacies of the two previous systems in providing bias currents at the collector-base junction as well as to the emitter-base junction. In the saturation region (transistor ON), the base voltage is greater than the collector voltage, and this produces forward bias on the collector-base junction.

Figure 6-4 represents the principal current flow paths associated with the transistor,

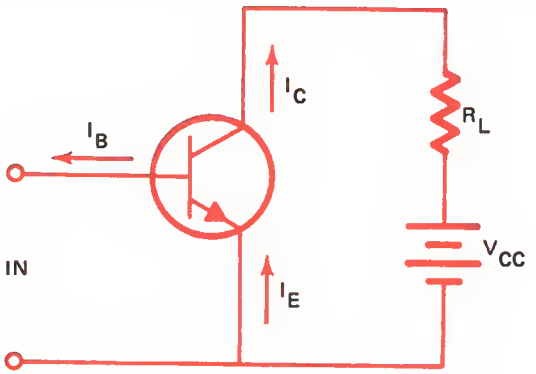


Fig. 6-4 Current Flow in the Transistor Switch

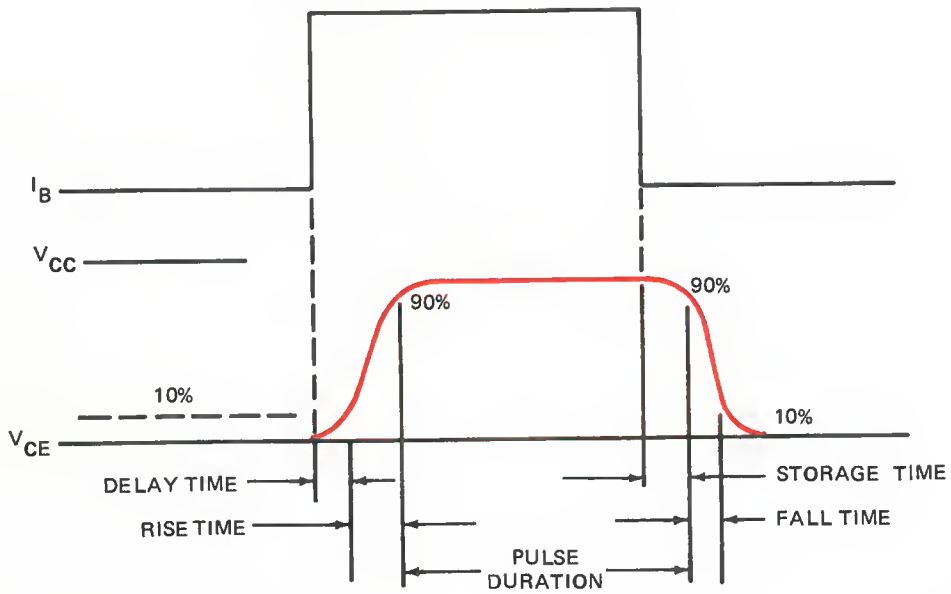


Fig. 6-5 I_B, V_{CE} Waveforms

remembering that $I_E = I_B + I_C$ in any transistor. Let's apply a pulse (see figure 6-5) to the base of the device. The I_B pulse is a pure square wave of current to the base. The resulting V_{CE} waveform shows what happens to the collector voltage. Important are the *delay time* (time required to reach 10%) at the beginning of the V_{CE} wave caused by the internal activities of the transistor, the *rise time* (between 10% and 90%) points on the leading edge of the curve, and the *fall time* (between 90% and 10%) on the trailing edge. One other time period needs explanation. This is the *storage time.* The storage time is on the trailing edge and is the time required for the curve to fall from 100% to the 90% point. This is often a significant time delay when the transistor is operated in the saturation region. When a transistor goes into saturation, the collector-base junction is forward biased, allowing carriers to flow into the base material. The switch cannot start from on to off until the extra carriers are removed from the base region to the collector. The time required to do this is called the storage time. It is represented actually by a time delay between removal of the I_B current and the effective start of the transistor turnoff. Thus, the device is said to have stored the I_B pulse for a short period of time.

The output waveform V_{CE} is not normally a truly faithful reproduction of the I_B waveform. Because of nonlinearities within all devices, it would be impossible to exactly reproduce any waveform. However, techniques do exist which allow much improvement in the transistor response. One common technique for shortening rise time is to use *base overdrive*, and a method of reducing storage time is to clamp the transistor so that is does not go very far into the saturation region. In extremely high speed switching applications, the device may be operated only to the extreme points of the active region on the loadline. This type of operation is quite complex and gives the lowest output for a given value of V_{CC}. Such operation is called full-driven operation.

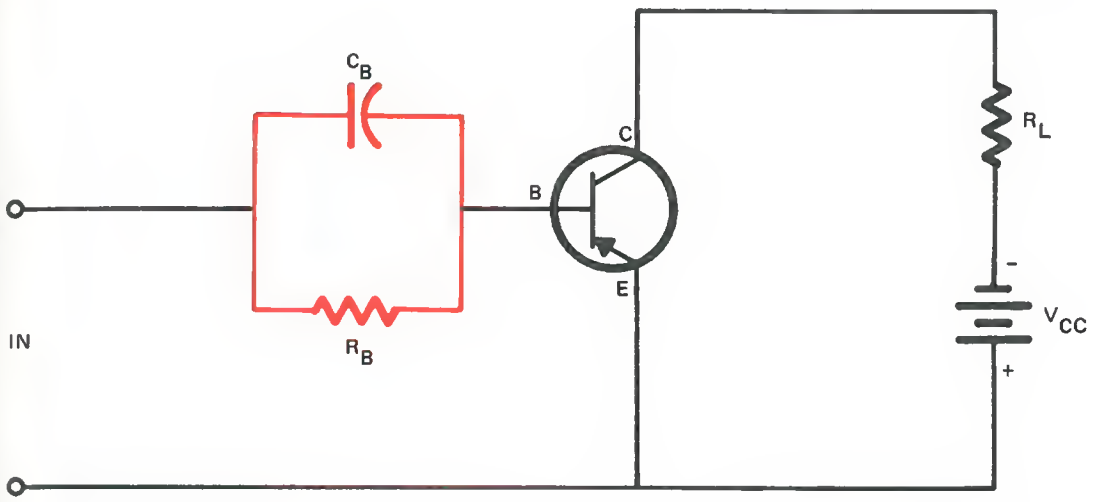


Fig. 6-6 Base Overdrive Circuit

A circuit for the base overdrive operation is shown in figure 6-6. This circuit provides a differentiated burst of current at the start of the pulse and thus speeds up the rise time. This seems a good system if we can determine values for R_B, R_L, and C_B.

One method of calculating these values is to utilize the transistor characteristic curves. The V_{BE} required for $I_{B\,on}$ can be determined with the input characteristic curve. $I_{B\,on}$ will either be given or it can be found by use of the output characteristic curves if V_{CC} is known. V_{BE} can be found as illustrated in figure 6-7. Once V_{BE} is known we can determine R_B by

$$R_B = \frac{\Delta V}{I_{B\,on}} \qquad (6.7)$$

ΔV is the difference between the maximum value of the input pulse and the $V_{BE\,on}$.

$$\Delta V = V_{in\,max} - V_{BE\,on} \qquad (6.8)$$

$R_B = \frac{\Delta V}{I_{B\,on}}$

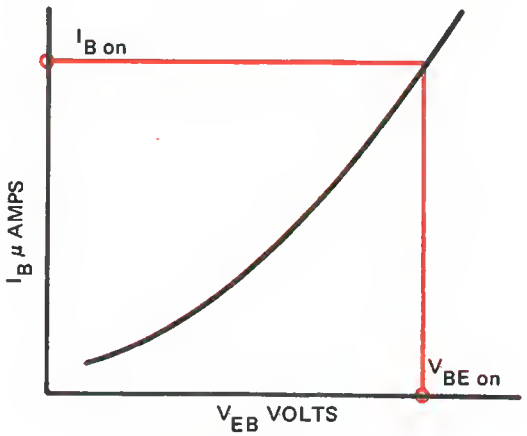


Fig. 6-7 Determining V_{BE}

Since the capacitor is to supply the desired overdrive current, the current I_{CB} through C_B will equal the $I_{B\ on}$ current.

$$I_{CB} = I_{B\ on} = \frac{C_B \Delta V}{\Delta t} \qquad (6.9)$$

Δt is the *desired* turn-on time. Solving this equation for C_B yields

$$C_B = \frac{I_{B\ on}\ \Delta t}{\Delta V} \qquad (6.10)$$

It is also possible to determine C_B experimentally. When R_B is in the circuit, different values of capacitance can be placed across it until the required rise time is obtained.

MATERIALS

- 2 Resistance substitution boxes (15Ω – 10 meg)
- 1 Transistor type 2N1305 or equivalent
- 1 Transistor socket
- 2 DC power supplies (0–40V)
- 1 Set of characteristic curves for 2N1305 transistor
- 1 Function generator
- 1 Capacitor substitution box

PROCEDURE

1. Using the transistor curves, calculate the required R_L for V_{CC} = 6V and I_C = 4 mA.
2. Construct the circuit shown in figure 6-8.

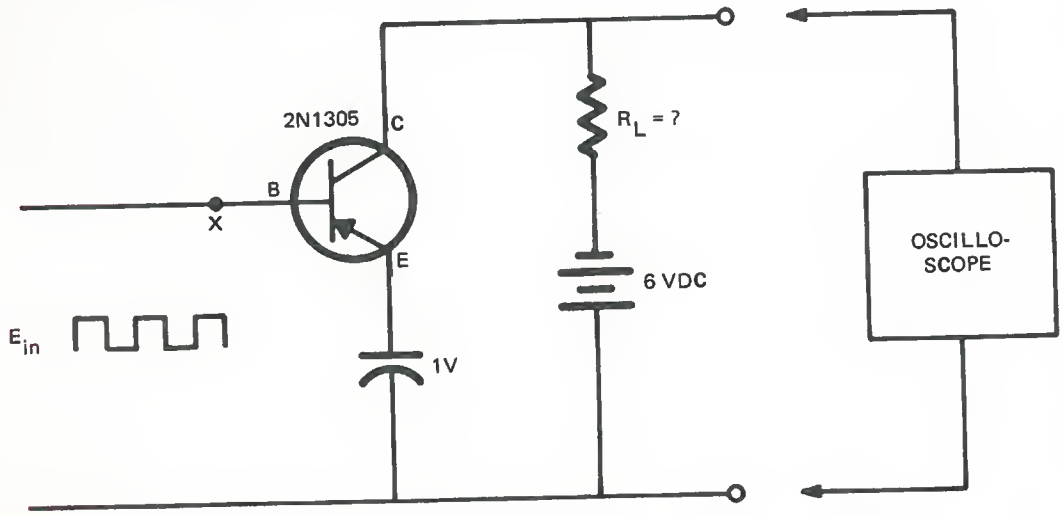


Fig. 6-8 The First Experimental Circuit

3. Apply a 2V peak-to-peak square wave to the base. Record the period, frequency, and pulse period of the input.
4. Observe the output on the scope.
5. Draw the wave shape carefully and label the appropriate parts: delay time, rise time, pulse duration, storage time, and fall time.

6. Measure and record each of the times in step 5.

7. Calculate R_B for a base overdrive circuit for the experimental circuit.

8. Wire the R_B into the experimental circuit as shown in figure 6-9.

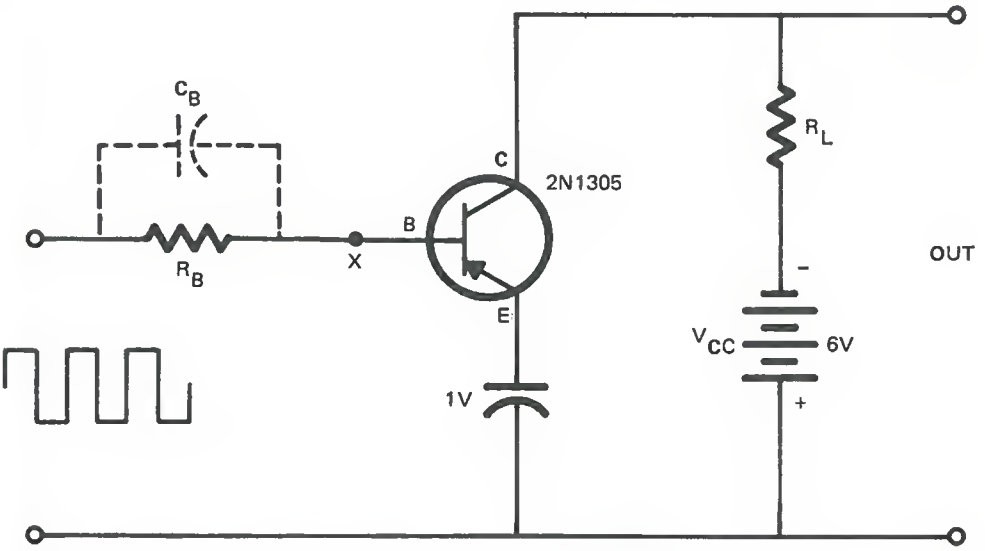


Fig. 6-9 The Second Experimental Circuit

9. Observe the output with the scope. Record the rise time, fall time and pulse duration. Carefully sketch the waveform.

10. Observe point X in the circuit of figure 6-9 with the oscilloscope. Measure and record rise and fall time. Carefully sketch the waveform.

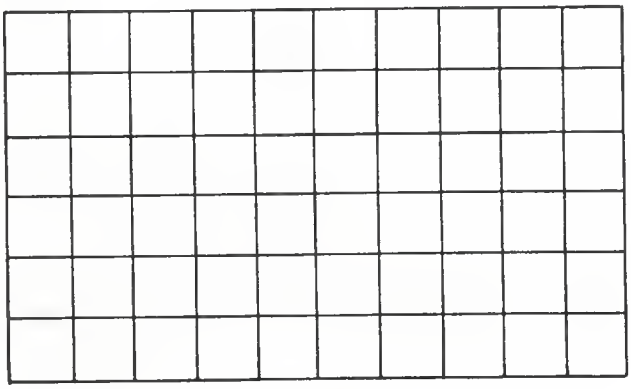
11. Calculate C_B for base overdrive of this circuit.

12. Install the appropriate C_B. Repeat steps 9 and 10.

13. Change the capacitance to a value three steps above and then three steps below the calculated C_B. Repeat steps 7 and 10 for each of these two new values.

ANALYSIS GUIDE. In analyzing these data, you should examine the parameters measured in the experiment and discuss their importance to switching applications. Contrast the calculated values with the values arrived at experimentally and comment on the accuracy of the calculation and empirical methods. The saturation and cutoff regions for this circuit should be identified on the characteristic curve.

CALCULATIONS R_L



Waveform

R_B CALCULATIONS

Fig. 6-10 The Data Tables

	DELAY TIME	RISE TIME	PULSE DURATION	STORAGE TIME	FALL TIME
FIRST CKT					
OUTPUT R_B					
POINT X R_B					
OUTPUT R_BC_B					
POINT X R_BC_B					
OUTPUT (Three Steps Above C_B)					
POINT X (Three Steps Above C_B)					
OUTPUT (Three Steps Below C_B)					
POINT X (Three Steps Below C)					

Output Waveform with R_B in the circuit

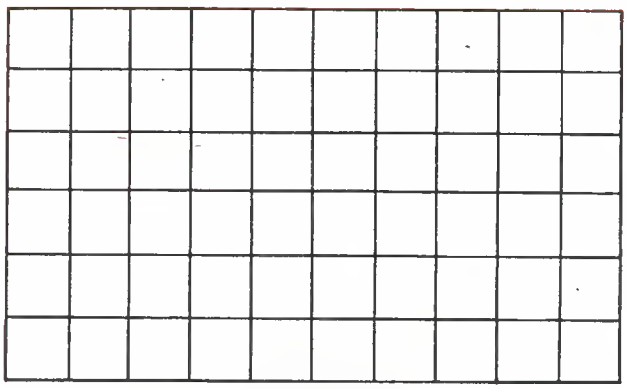
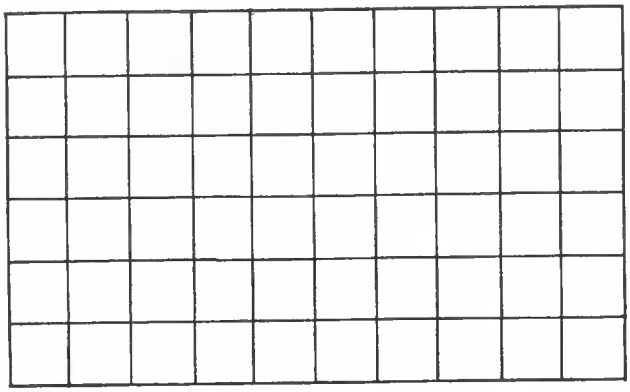


Fig. 6-10 The Data Tables (Cont.)

Waveform at Point X with R_B in the Circuit



C_B CALCULATIONS

Output Waveform with C_B in the Circuit

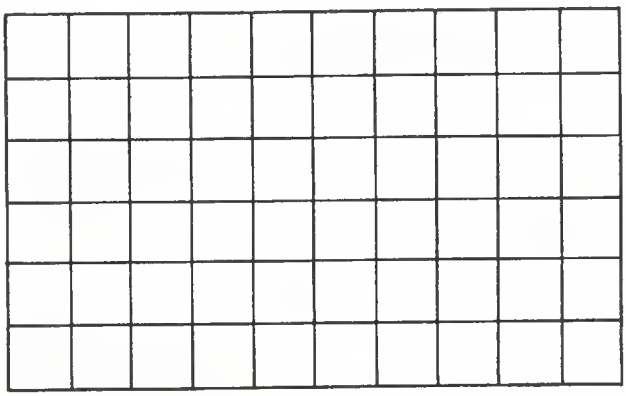
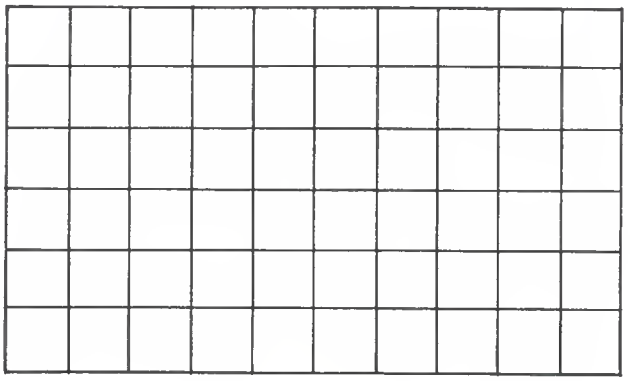
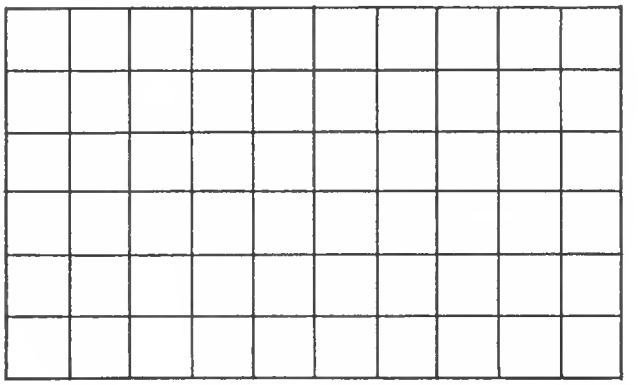


Fig. 6-10 The Data Tables (Cont.)

Waveform at Point X with C_B in the Circuit



Output Waveform with C Three Steps Above C_B



Waveform at Point X with C Three Steps Above C_B

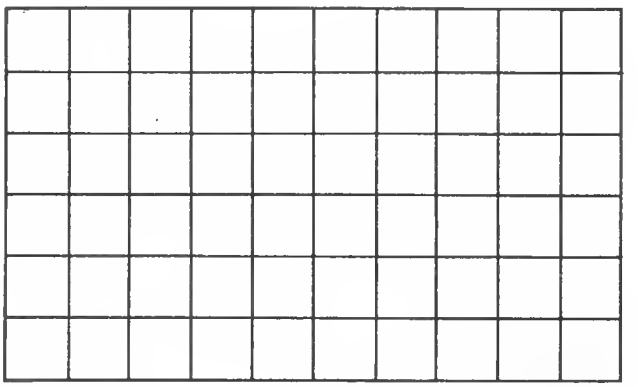
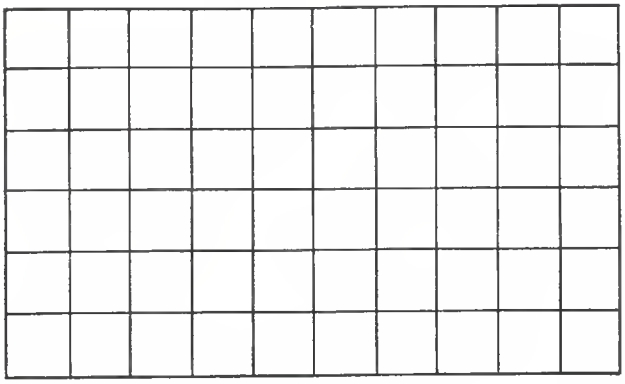


Fig. 6-10 The Data Tables (Cont.)

Output Waveform With C Three Steps Below C_B



Waveform at Point X With C Three Steps Below C_B

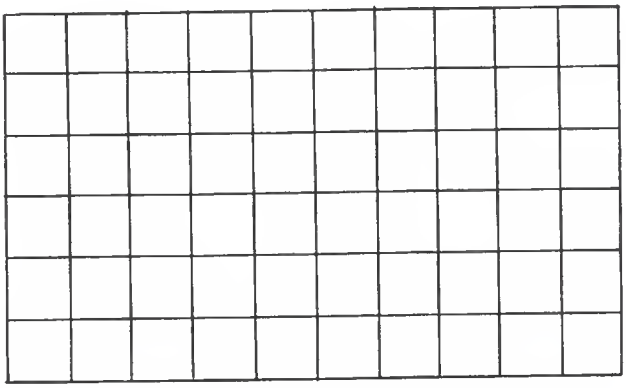


Fig. 6-10 The Data Tables (Cont'd)

PROBLEMS

1. Calculate saturation I_C for a transistor operated with V_{CC} = 30V and the R_L = 1800Ω.
2. Draw the equivalent circuit for a transistor in the saturation region. Explain your reasons for thinking it to be reasonable.
3. Draw the equivalent circuit for a transistor in the cutoff region. Explain why you think your circuit is reasonable.

experiment 00111 DIODE CLIPPERS

INTRODUCTION. The diode is frequently encountered in logic circuits. In this experiment we will examine some of the ways that this device is used to perform the job of adjusting and polarizing an input signal.

DISCUSSION. Diodes and transistors are both used to "sort out" pulses for input to digital circuits. These devices can be used in different circuit configurations to polarize and set the level of input pulses. They can also help shape a waveform by "trimming" off unwanted spikes and transients.

The first circuit we will look at is a series clipper. This circuit should be familiar to you as a half-wave rectifier. A simple series clipper circuit is shown in figure 7-1. Only the positive going pulses (or the negative going if the diode is reversed) will be passed by the forward biased diode D_1. Using Ohm's Law, we can write an equation for the circuit parameters where E_{in} is the peak amplitude of the square wave input voltage, I_f is the forward diode current, R_f is the forward diode resistance, and R_L is the load resistance. The equation for the positive half cycle of the input wave with the diode positioned as shown is

$$E_{in} = I_f (R_L + R_f) \qquad (7.1)$$

A similar equation can be written for the negative half cycle.

$$E_{in} = I_r (R_L + R_r) \qquad (7.2)$$

E_{in} and R_L are the same as before, but I_r is the reverse current of the diode while R_r is the reverse resistance of the diode. It is important that the *front-to-back resistance ratio* of the diode be relatively large. It is also desirable that the reverse resistance of the diode be much larger than R_L and also R_L be much larger than the forward resistance of the diode. ($R_r << R_L >> R_f$).

The circuit shown in figure 7-1 is used only for clipping pulses at the zero level. If some other clipping level is desired, the ad-

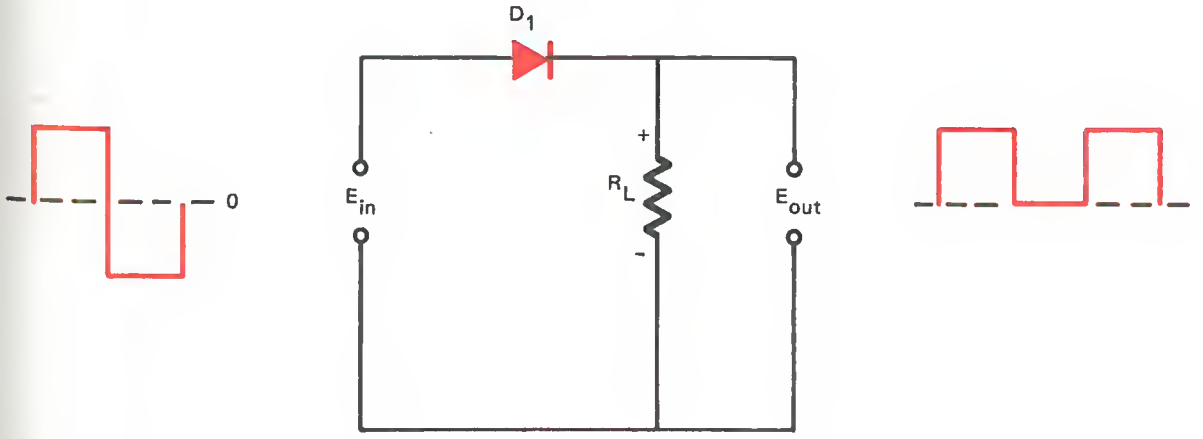


Fig. 7-1 Series Diode Clipper

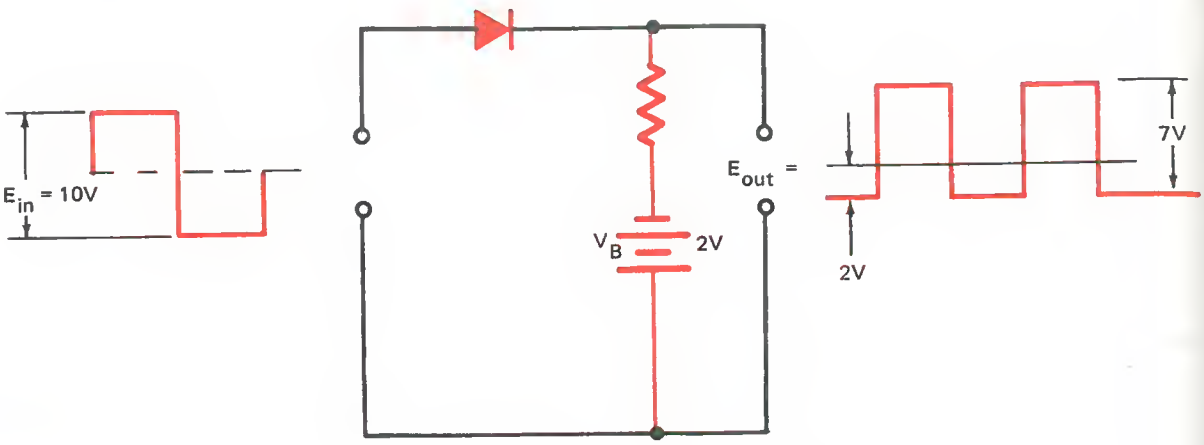


Fig. 7-2 Forward Biased Diode Clipper

dition of a series bias voltage is necessary. By choosing the voltage properly, various levels can be selected. Figure 7-2 shows a forward bias applied to the previous circuit. With this configuration, the output will be 7V clipped. The two-volt bias battery voltage adds to the original 5V clipped output.

In the circuit of figure 7-3, the opposite effect is achieved by reverse biasing the diode with two volts. The output then becomes 3 volts clipped.

In the case of figure 7-2, the negative 2V causes the forward current to increase. Actually, the diode is forward biased when the input voltage is greater than –2V and until it reaches +5V. In the second case (figure 7-3), the diode is reverse biased at 2 volts. This 2 volts must be overcome for the diode to reach the original 0V bias level. Thus, 2 volts of the E_{in} value are required to reach the zero level and the output is the 3V that are left.

We have seen the effect of a series diode. What would happen if the diode were in *parallel* with R_L? Figure 7-4 shows such a circuit. A series current-limiting resistor is often added to protect the diode from exces-

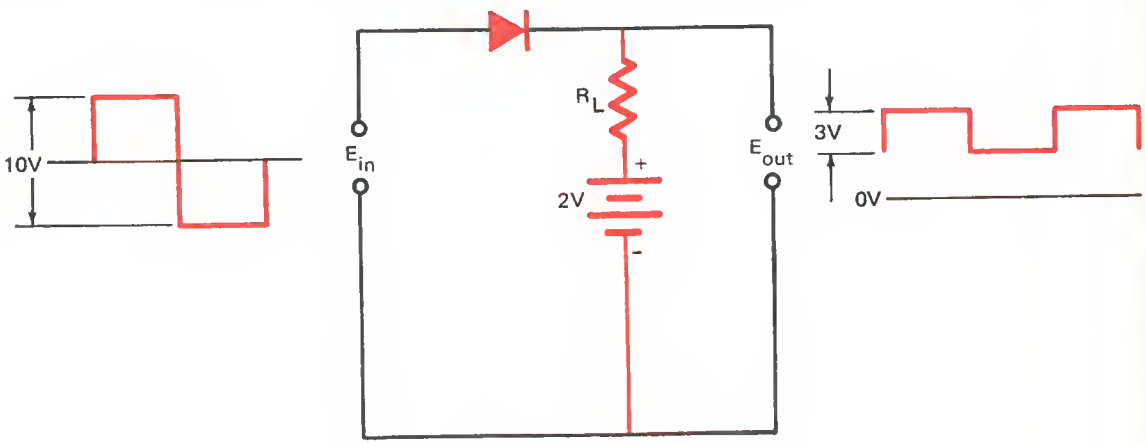


Fig. 7-3 Reverse Biased Diode Clipper

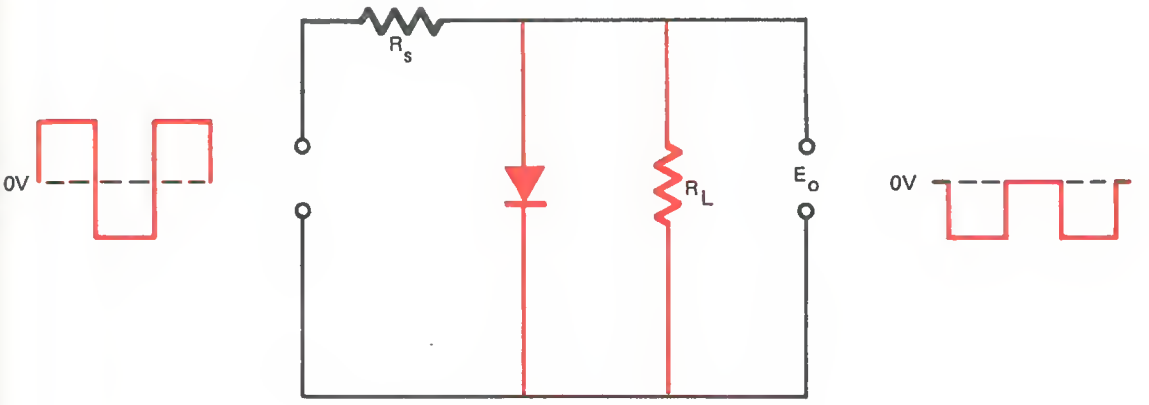


Fig. 7-4 Unbiased Shunt Diode Clipper

sive current during the conduction. During conduction (positive half cycle of E_{in}) the forward resistance of the diode must be very much smaller than the value of R_L. If this is the case, the diode leg of the circuit will effectively short the positive half cycle to ground. During the negative half cycle, the reverse resistance of the diode should be much greater than R_L. The current through R_L will produce E_o as a negative pulse. In the design of these circuits, the resistance relationships are important. The reverse resistance of the diode should be by far the highest resistance in the circuit. The load resistance is the next largest. The series resistance is much lower than R_L, and the forward resistance of the diode should be the smallest of all. The differences between these values should be many thousands of ohms.

As with the series clipper, the shunt clipper can be both forward and reverse biased to produce different clipping levels. This happens just as it does in the series circuit in that the clipping occurs during the conduction time of the diode because the bias alters the conduction of the diode. Figure 7-5 shows this action in a reverse biased shunt clipper. The output will be the full amplitude of the negative half cycle of the input. The positive portion of the waveform will be equal to the positive value of the

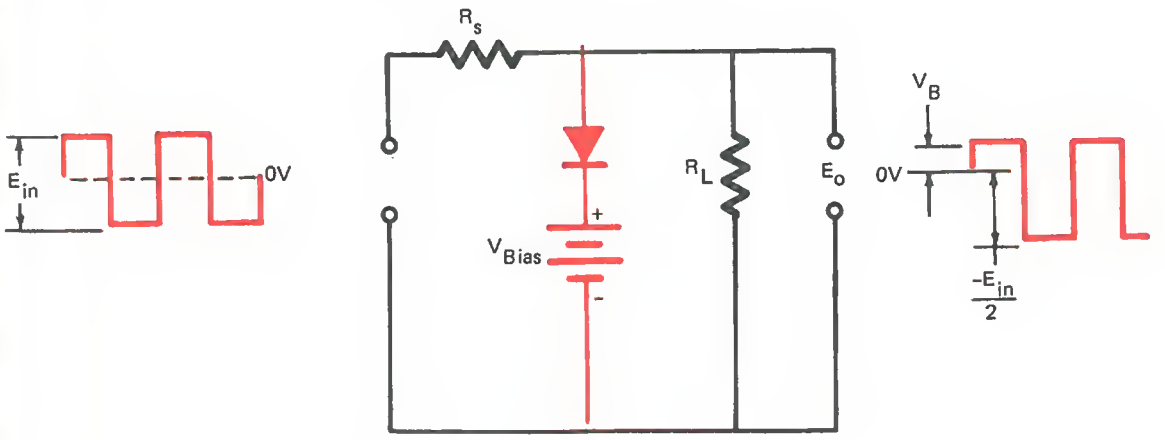


Fig. 7-5 Reverse Biased Shunt Diode Clipper

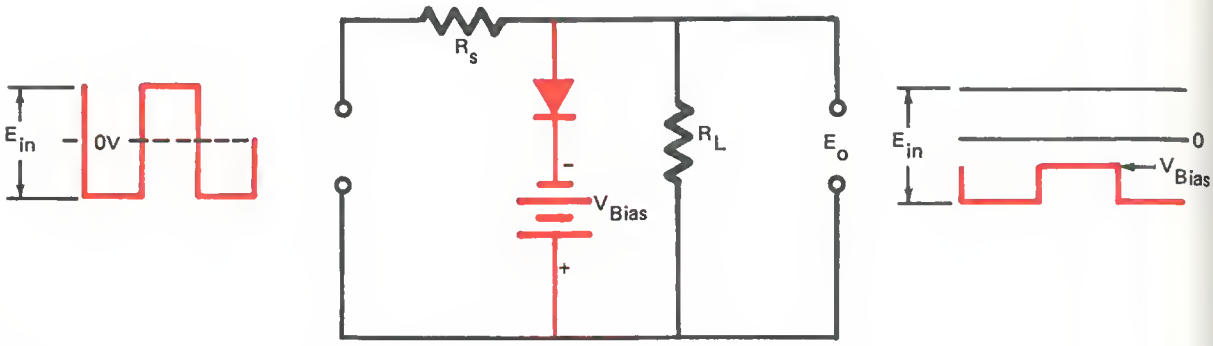


Fig. 7-6 The Forward Biased Shunt Diode Clipper

bias voltage. This happens because the diode conducts any time the input voltage is greater than the reverse bias. The forward resistance of the diode must be much smaller than R_s, and R_L must be much greater than R_s. The forward current through the diode during conduction is then

$$I_f = \frac{E_{in} - V_{Bias}}{R_s} \text{ if } R_s >> R_f \qquad (7.3)$$

where the V_{in} is the positive half cycle of E_{in}. During this half cycle, the output voltage is equal to the bias voltage. It can be seen from this discussion that the addition of reverse bias to the shunt clipper actually reduces the clipping action.

Forward biasing of a shunt clipper circuit is shown in figure 7-6. This configuration increases the clipping action. When we forward bias the diode, we allow conduction through the major portion of the input voltage cycle. Only that portion of E_{in} which is negative and greater in magnitude than V_{Bias} will appear across R_L.

There is one other type of shunt diode clipper that is useful. It is the double shunt diode clipper. This circuit is used in many square wave generators. Figure 7-7 shows a typical double shunt circuit. The sine wave input is "squared" by the clipping action of the diodes. The more severe the clipping action, the more nearly square the output. Both diodes are reverse biased. These biases are equal when the square wave is symmetric. When D_1 conducts, the output wave will rise to the bias voltage value of V_{B1}. When D_2 conducts, the output voltage will go negative, to the value of V_{B2}. So D_1 clips the positive half cycle of E_{in}, and D_2 clips the negative half cycle of E_{in}.

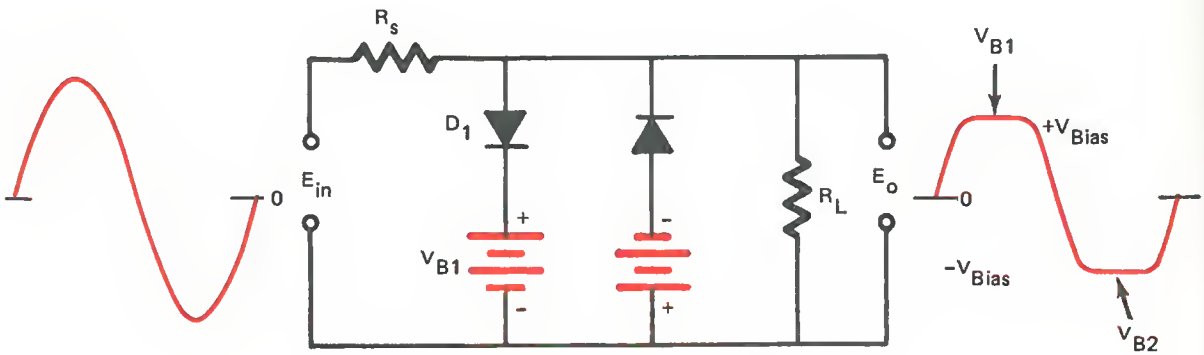


Fig. 7-7 Double Shunt Diode Clipper

MATERIALS

1 Diode, 1N645 or equivalent
2 Resistance substitution boxes (15Ω - 10 meg)
1 DC power supply (0–40V)
1 Oscilloscope
1 Function generator
1 Breadboard with terminals

PROCEDURE

1. Assemble the circuit shown in figure 7-8.

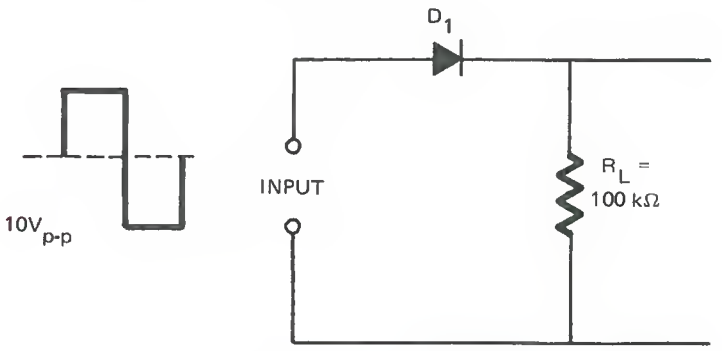


Fig. 7-8 The First Experimental Circuit

2. Apply a 1 kHz, 10 V_{p-p} square wave to the input terminals of the clipper.
3. Connect the oscilloscope across R_L and sketch the output waveform. **Be sure to record the amplitude, period, and zero reference level.**
4. Add the 2V bias as shown in figure 7-9.

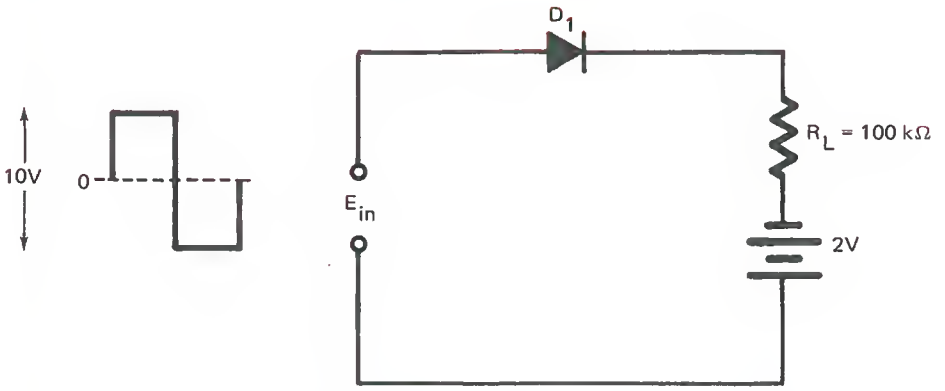


Fig. 7-9 The Second Experimental Circuit

5. As before, measure, record, and sketch the waveform across R_L with a 5 V_{p-p}, 1 kHz input square wave signal applied.
6. Reverse the leads to the 2V bias supply.

7. Measure, record, and sketch waveform data as before.
8. Disassemble the circuit and construct the circuit shown in figure 7-10.

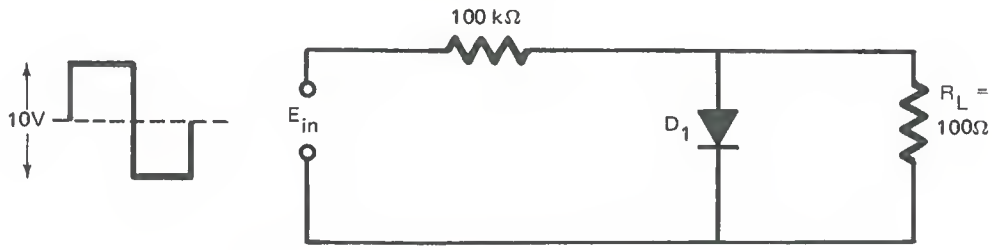


Fig. 7-10 The Third Experimental Circuit

9. Apply a 5 $V_{p\text{-}p}$, 1 kHz square wave signal across the input.
10. Measure, record and sketch the waveform across R_L.
11. Add the 2V bias shown in figure 7-11.

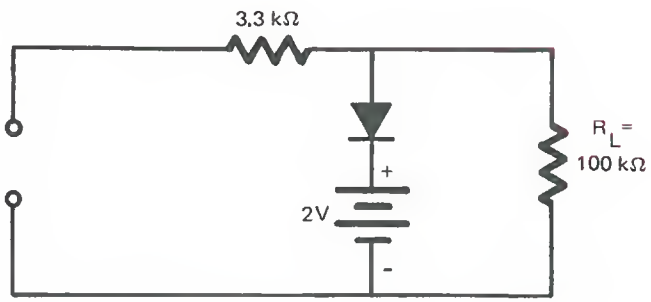


Fig. 7-11 The Fourth Experimental Circuit

12. With the 5 $V_{p\text{-}p}$, 1 kHz pulses applied, measure, record, and sketch the waveform across R_L.
13. Reverse the polarity of the bias supply.
14. Repeat step 12.

ANALYSIS GUIDE. In analyzing your results, you should explain how the levels of clipping in the individual waveforms were achieved. The action of the series and shunt clipper should be explained using your data.

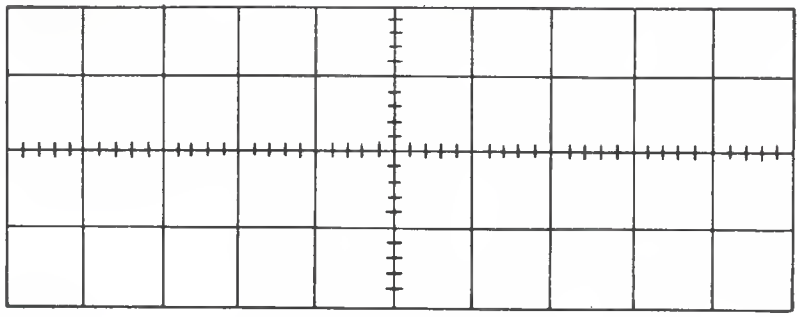
PROBLEMS

1. Calculate the forward diode current in the Fourth Experimental Circuit, Step 12.
2. A certain diode has a reverse resistance of 10 megohms. Its forward resistance is 10 ohms. Select R_s and R_L for a forward bias clipper biased at -3V.
3. Draw a double shunt clipper. If $V_{Bias\ 1} = +2V$ and $V_{Bias\ 2} = -3V$, what will be the total voltage swing of E_{out}?

First Circuit

Amplitude = _____

Period = _____

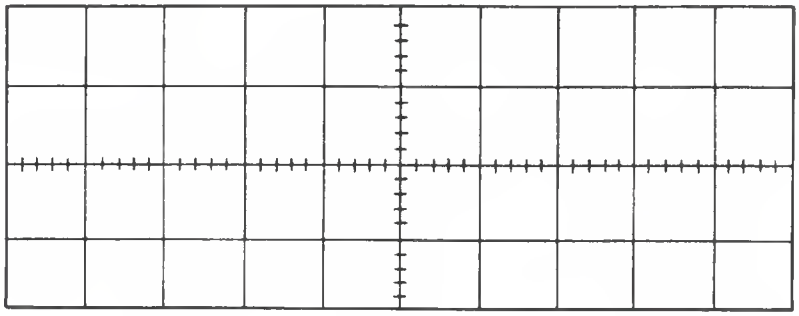


Output Waveform
(Show zero reference level)

Second Circuit

Amplitude = _____

Period = _____

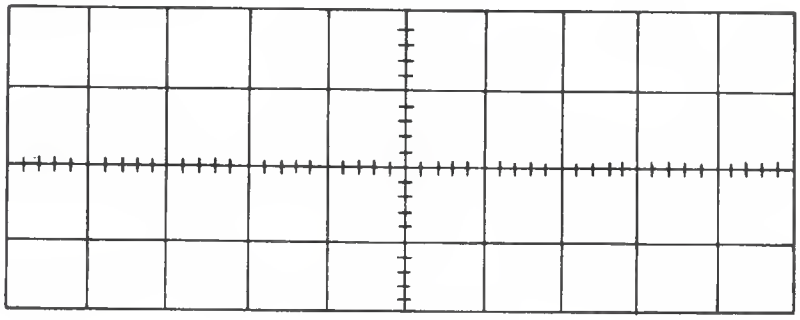


Output Waveform
(Show zero reference level)

Third Circuit

Amplitude = _____

Period = _____



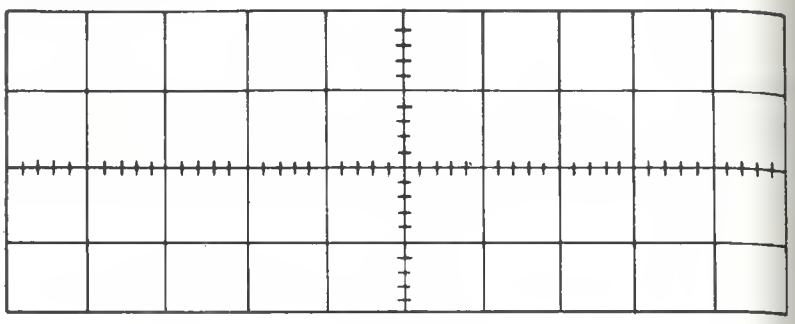
Output Waveform
(Show zero reference level)

Fig. 7-12 The Data Tables

Fourth Circuit

Amplitude = _____

Period = _____



Output Waveform
(Show zero reference level)

Fig. 7-12 The Data Tables (Cont'd)

experiment 01000 TRANSISTOR CLIPPERS AND CLAMPS

INTRODUCTION. Most semiconductor devices can be used in wave and pulse selection. The transistor, like the diode, can be used for clipping and clamping waveforms. In this experiment we will examine how a transistor is used for clipping, and what is meant by clamping and how it is achieved.

DISCUSSION. A method for obtaining square waves in many practical systems is to "square" a sine wave. This can be done in several ways with both transistors and diodes. In this experiment we will look at how this can be done.

The first circuit we shall consider is called a transistor clipper, its schematic is shown in figure 8-1. This circuit takes advantage of the cutoff characteristics of the transistor. Actually the transistor is driven into both saturation and cutoff, which in a class A design would be called distortion due to overdriving. In this case if the input signal is sufficiently large in amplitude, the sides of the sinewave will be almost (but not quite) perpendicular, and when the transistor reaches its maximum (or minimum) signal capability the voltage waveform is said to be "clipped." The load resistance and the saturation voltage are the only really critical parameters for the transistor clipper. Equation 8.1 will yield the value of the load resistance.

$$R_L = \frac{V_{CC}}{I_{C\ max}} \qquad (8.1)$$

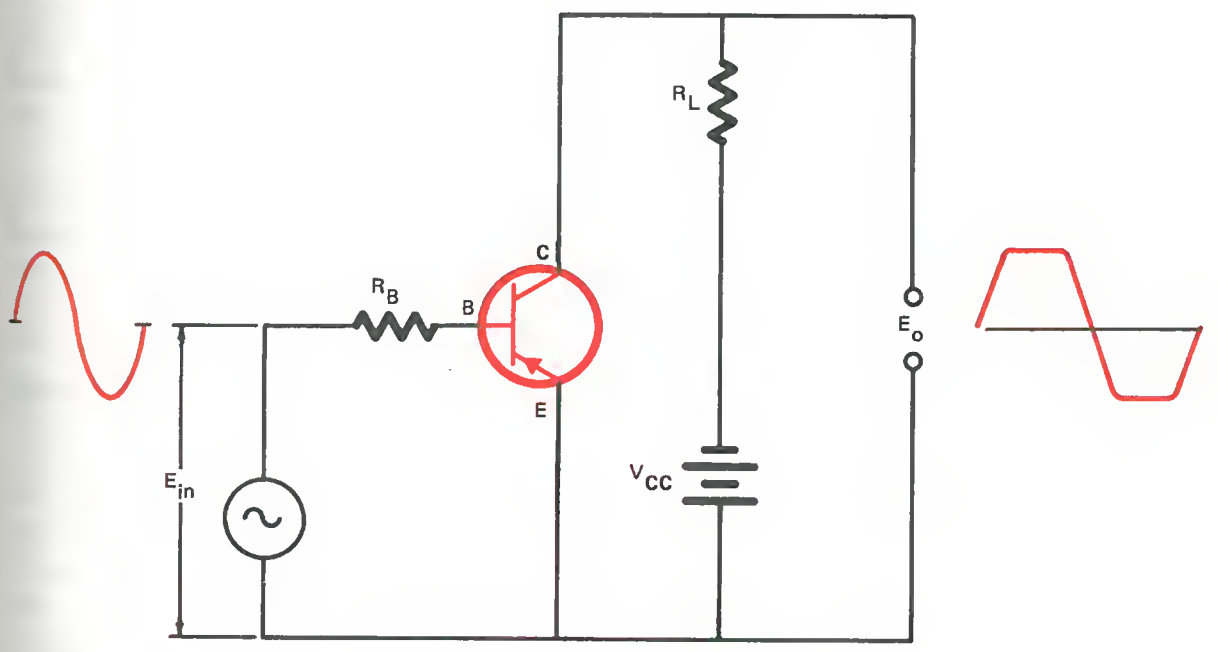


Fig. 8-1 The Transistor Clipper

This equation is used to lay out the DC load line. V_{CC} is the collector supply voltage. I_C is the maximum saturation collector current. This is illustrated in figure 8-2 where the load line is drawn from the collector supply voltage V_{CC} to I_C maximum. The $I_{B\ SAT}$ (base current for saturation) can be found where the saturation knee of the characteristic curve intersects the load line. The input voltage for saturation can be found by

$$E_{in\ SAT} = R_B I_{B\ SAT} \qquad (8.2)$$

Actually of more importance from the design standpoint is the value of the base resistor R_B which also appears in equation 8.2. I_B for saturation can be taken from the characteristic curve once the load line is drawn. The task then is to balance the E_{in} for saturation against the R_B to swing the base waveform from cutoff to saturation. The transposition of 8.2 will give the form for selecting R_B.

$$R_B = \frac{E_{in\ SAT}}{I_{B\ SAT}} \qquad (8.3)$$

The desired action of this circuit is simply *on and off* at the frequency of the input sinewave, that is, an output square wave of the same frequency. At the start with no signal at the base, the transistor is off and the collector is at its supply voltage. After applying the signal, the negative half cycle drives the transistor to saturation, decreasing the output voltage value to almost zero. During the positive half of the input cycle the input is reverse-biased and the output remains off. When the input signal reaches $E_{in\ SAT}$, the transistor is on and the voltage at the collector goes almost to zero.

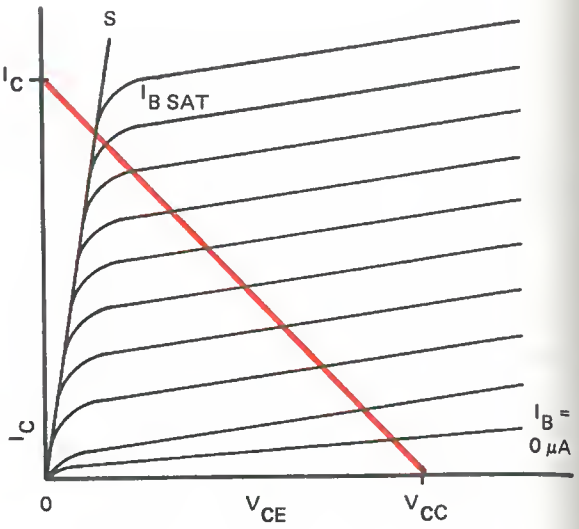


Fig. 8-2 Clipper Load Line

The *rise* and *delay times* are determined from the time required for the base current to reach the saturation level. The base emitter resistance will usually be negligible when compared to R_B, so the base current becomes

$$I_B = \frac{E_{in}}{R_B} \qquad (8.4)$$

The input voltage for saturation is the voltage across R_B (equation 8.3). The rise time (and fall time) can be determined using the expression

$$E_{in\ SAT} = V_{max} \sin 2\pi ft \qquad (8.5)$$

Both the load resistor and the base resistor have an influence on the rise and fall times. The base current required for saturation is established by the load resistor, while the base resistance determines the level of input voltage required to produce the base saturation current.

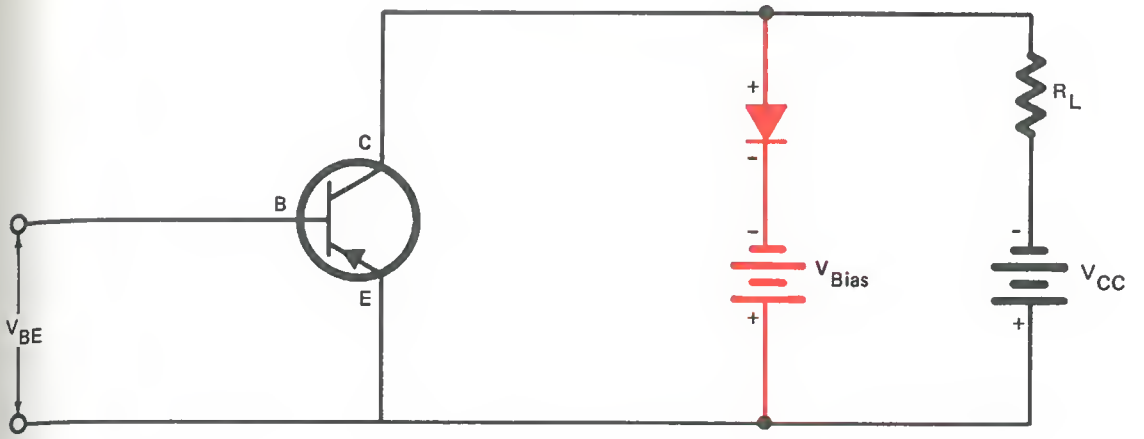


Fig. 8-3 Diode Collector Clamp

The effect of the input frequency is to cause a decrease in rise and fall times with an increase in frequency. The end limit of this trend is the value of the transistor switching time. The problem of switching time frequently arises in transistor switch applications. It may seem strange that with a device as rapid as the transistor we would be so concerned with how long it takes to switch. However, when you consider the millions of switching operations that a computer must make in relatively short periods of time, very fast action is indeed required.

The turn-off time of a transistor switch is increased when the device is allowed to go deep into saturation. Anytime the collector-base junction is forward biased, majority carriers are allowed to pass into the base region. These carriers must be removed in order to turn the transistor off. This condition worsens as the device is driven further and further into saturation. In other words, the turn-off time becomes a function of the degree of saturation. It is sensible that the best way to prevent this is to prevent the transistor from going deep into saturation. In order to do this we can use what is called a diode clamp. This clamp will not allow the collector voltage to drop beyond a predetermined level. By setting this level properly we will be able to hold the ON operating point just inside the active region. The collector-base junction will never become forward biased and the majority carriers will not tend to fill up the base region. With few majority carriers to remove, the device is ready to switch OFF once the signal is removed and the turnoff time is considerably reduced.

Examination of figure 8-3 will more clearly demonstrate the diode collector clamp idea. In this circuit the supply voltage is

$$V_{CC} = V_{Bias} + \text{The forward drop of the diode} \quad (8.6)$$

which says that the $V_{CC\ ON}$ voltage will never decrease below the value of the diode forward drop added to its own bias voltage. This gives us a method for setting the collector clamp voltage. The object is to prevent the base-collector from becoming forward biased. This means that the bias voltage must be chosen such that the conducting collector-emitter drop is always much larger than the base-emitter voltage. The

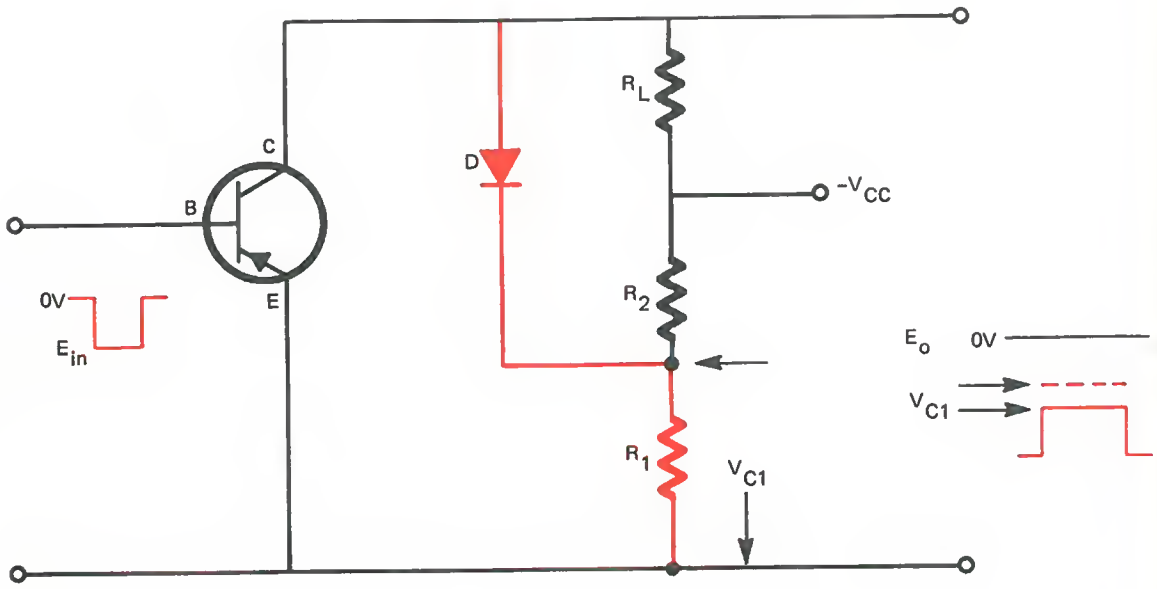


Fig. 8-4 Practical Diode Collector Clamp

diode is at cutoff except when the collector-emitter voltage decreases to the diode bias voltage level. At that point the diode conducts and decreases the collector-emitter voltage to the value of the diode bias plus the forward drop of the diode. The proper value of the diode bias voltage can be determined by selecting voltages so that $E_{CE\ ON}$ is much larger than E_{BE}. Then

$$V_{CE\ ON} = V_{Diode\ FD} + V_{Bias} \qquad (8.7)$$

or

$$V_{Bias} = V_{Diode\ FD} - V_{CE\ ON} \qquad (8.8)$$

A more practical circuit for diode collector clamping is shown in figure 8-4. The collector clamping level is set by the voltage divider R_1 and R_2. This level is the value

$$V_{C1} = \frac{V_{CC}R_1}{R_1 + R_2} \qquad (8.9)$$

When no signal is present at the base, the output rises to the clamp potential V_{C1}.

Several problems develop with this circuit although it is better than a saturated switch. First of all, the recovery time of the diode is a limiting factor. The circuit can never be faster than the diode recovery plus circuit recovery. The second drawback is that the circuit wastes current and this current must be dissipated by the transistor. I_C is still at its maximum value and the extra portion is diverted through the diode.

Other techniques exist for the design of nonsaturated switches that, in part, overcome the disadvantages of our simple collector clamp. One way to accomplish this is to control I_B and thereby control I_C. This approach is used in the signal-diode back clamp shown in figure 8-5. This circuit is particularly useful when employing base overdrive. To improve the output square wave saturation, I_B is supplied by the overdrive circuit. V_{CE} begins to decrease toward zero as it reaches the value of E_{in} (the drop across R_s). The diode will conduct because of the change in the bias. This will let part of I_B go around the overdrive circuit and the

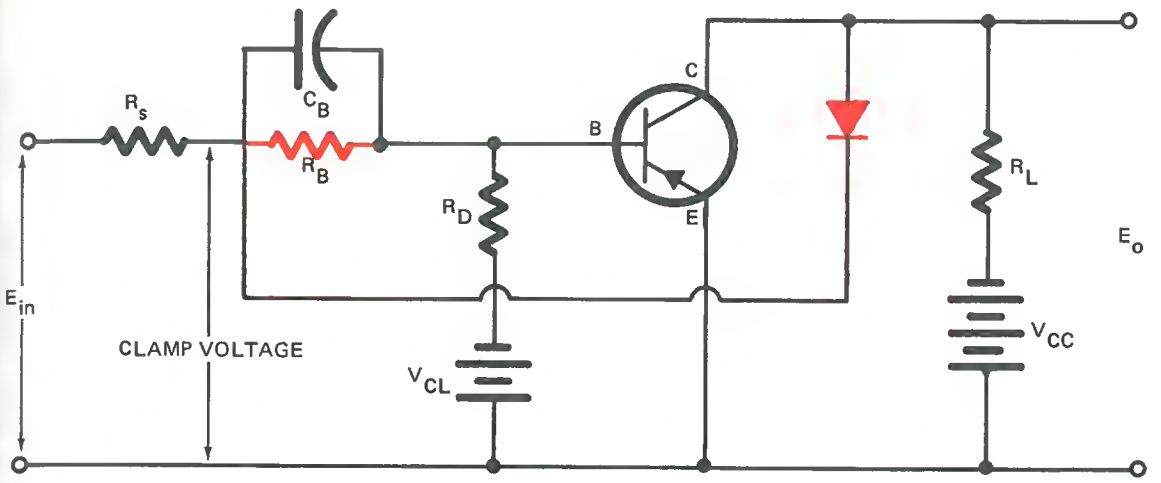


Fig. 8-5 Single Diode Back Clamp

transistor (a sort of bypass relief valve). This I_B will oppose the incoming I_C and prevent it from rising beyond that instantaneous value. The collector current I_C is equal to the β_f of the transistor plus the excess I_B in the bypass. The current through the load resistor will be more-or-less constant and equal to $\beta_f I_B$. The clamp voltage is set by the value across R_s in conjunction with E_{in}. In order to choose the clamping voltage, we can use

$$V_{clamp} = V_{CE}\text{ (desired)} + V_{\text{forward drop across diode}} \quad (8.10)$$

Since the diode is not directly across the output, its recovery time does not seriously affect the circuit.

Another approach for collector clamping is a slightly modified version of figure 8-5 employing two diodes. Such a double diode clamp is shown in figure 8-6. This circuit has all the same parts as the previous one except that the base series overdrive resistor has been placed with a silicon diode. A silicon diode was chosen here because of its characteristic voltage drop (from 0.5V to

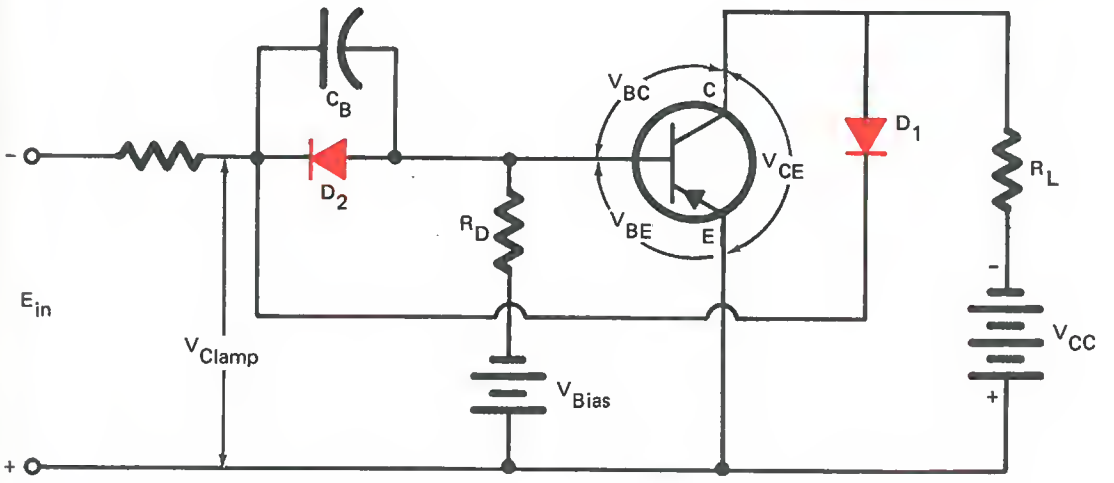


Fig. 8-6 A Double Diode Clamp

0.7V) in the forward direction. In this circuit the diode is always forward biased. The diode D_1 at the collector is a germanium type and is reverse biased until the collector-emitter voltage tries to drop below the clamping voltage. At that point, D_1 conducts with a forward drop of approximately 0.2 volts. This excess base current opposes I_C and prevents any further drop of V_{CE}. With the transistor conducting, V_{CE} can be determined by

$$V_{CE} = \text{Forward Drop } D_1 + \text{Clamp Voltage} \quad (8.11)$$

With the transistor off, V_{BC} is

$$V_{BC} = \text{Forward Drop } D_2 + \text{Voltage Across } D_1$$

With the transistor on

$$V_{BC} = \text{Forward Drop } D_2 + \text{Forward Drop } D_1 \quad (8.12)$$

and the base-emitter voltage is

$$V_{BE} = \text{Forward Drop } D_2 + \text{Clamp Voltage} \quad (8.13)$$

The transistor cannot enter the saturation region when the conducting value of V_{CE} is greater than V_{BE} at the time. Substituting, we can observe that the forward drop of D_1 plus the clamping voltage must always be greater than the value of the forward drop of D_2 plus the clamp voltage. The trick here is that the equation

$$V_{D1} + V_{Clamp} > V_{D2} + V_{Clamp}$$

has its implications obscured by the fact that both V_{D1} and V_{D2} are opposing the clamping voltage. Since we chose D_2 as a silicon diode, we insured that its forward drop would oppose the clamp voltage in the base circuit and this always makes the conducting value $V_{CE} > V_{BC}$.

MATERIALS

- 1 Oscilloscope
- 1 Function generator
- 1 DC power supply (0-40V)
- 1 Transistor type 2N1305 or equivalent
- 1 Output characteristic curve for the transistor
- 3 Resistance substitution boxes (15Ω - 10 meg suitable selection of resistors)
- 1 Transistor socket
- 1 Breadboard
- 1 6.8 kΩ resistor 1/2W
- 1 VOM or FEM
- 1 Diode type IN305 or any other germanium type
- 1 1 kΩ resistor 1/2W

PROCEDURE

1. Calculate R_B and R_L for a transistor clipper with a 2N1305 transistor operating at V_{CC} = 6V. (Choose I_B = 200 μA and I_C = 4 mA.)
2. Construct the circuit shown in figure 8-7.

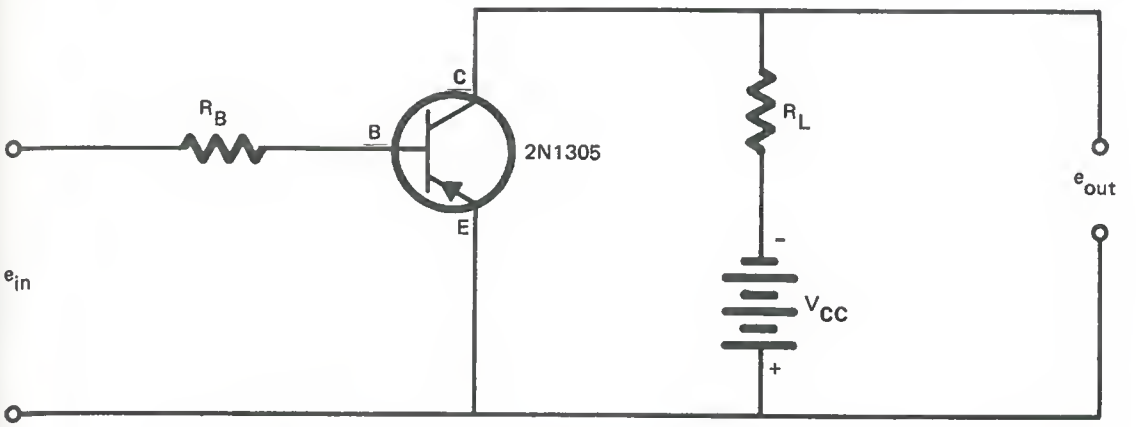


Fig. 8-7 The First Experimental Circuit

3. From the function generator, apply a 10V peak sine wave at 1 kHz.
4. Observe and record the output waveform.
5. Measure and record the rise time of the leading and trailing edges.
6. Measure and record e_{in} and I_B.
7. Calculate the rise time for the leading and trailing edges.
8. Disassemble the circuit.
9. Calculate the values of R_L, R_1 and R_2 for a practical diode collector clamp.
10. Assemble the circuit shown in figure 8-8.

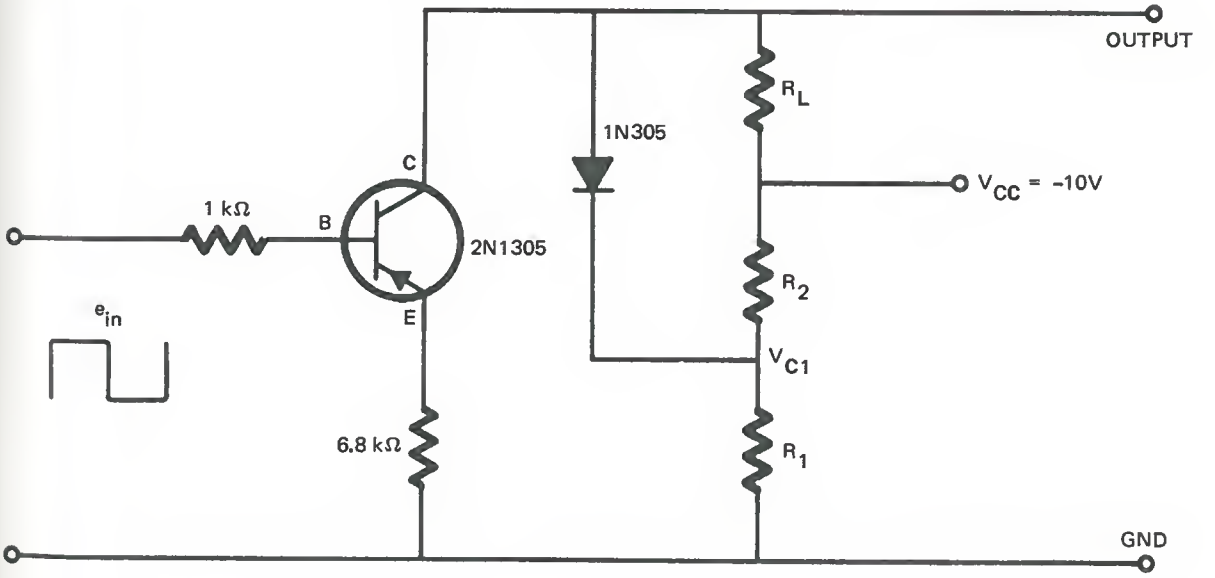


Fig. 8-8 The Second Experimental Circuit

	R_B	R_L	V_{CC}	I_B	E_{in}	tLE	tTE
Calculated							
Measure							

Output Resistor Clipper

	R_L	R_2	R_1	V_{CC}	V_{C1}	E_{in}
Calculated						
Measure						

Output Diode Emitter Clamp

Fig. 8-9 The Data Tables

11. Apply a 5 $V_{p\text{-}p}$, 1 kHz square wave at the input terminals.
12. Observe the output on an oscilloscope. Record the waveform. Record the amplitude of the square wave.
13. Measure and record V_{C1}.

ANALYSIS GUIDE. The purpose of this experiment has been to become familiar with clipping and clamping in transistor circuits. You should discuss how this is done in a variety of circuits. Why is it done? Which of the circuits that you investigated was the best? Why do you think so? Could the transistor circuit in figure 8-1 be used with a square wave input?

PROBLEMS

1. Given a collector clamp with a silicon diode and a bias voltage of 3 volts, what is the clamp voltage V_{CE}?
2. Given a single diode back clamp with an I_C required at 6 mA and the current through the load resistor 3 mA, how much current will pass through the diode?
3. We wish to build a double diode clamp. The voltage collector-to-emitter with the transistor conducting is 1.5 volts. The diode D_1 is germanium and has a forward drop of 0.2V. We wish to clamp the collector at 6V. Is this possible? Explain your answer.

experiment 01001 DIODE LOGIC GATES

INTRODUCTION. *Gates* are used to control the selection of logic pulses. In this experiment we shall examine how diodes are used as logic gates.

DISCUSSION. Logic gates, like all logic circuits, normally operate with two possible input levels. These inputs are signals that represent "true" or "false", OFF or ON, or the digits of the binary number system. The two signal levels could be represented by any two voltage levels. When the more positive level represents the binary 1 or "yes", the logic system is termed *positive logic.* In positive logic, the more negative level represents 0 or "no". When the more negative level is a 1 or a "yes", the logic system is termed *negative logic.* The levels can be of different polarities or the same polarity so long as one is more negative or more positive than the other. There are many different types of systems in use today. Some of the most popularly used levels seem to be –11 and –3, –10 and 0, –6 and 0, and –5 and 0 volts.

A diode gate consists of two or more input terminals with a semiconductor diode in series with each. Basically, there are two types. They correspond to the two Boolean operations, OR and AND. (We also frequently call them plus (+) and times (X).) Figure 9-1 shows both types of gates. Notice that the polarity of the diodes are reversed.

In the case of the OR gate, when any one of the gates receives a signal, the gate produces an output. That is, an output pulse exists when any or all of the input signals are present at A, or B, or C. The Boolean equation for the circuit shown is

$$A + B + C = \text{Output} \qquad (9.1)$$

OR gates will operate for any number of inputs as long as the inputs are more positive

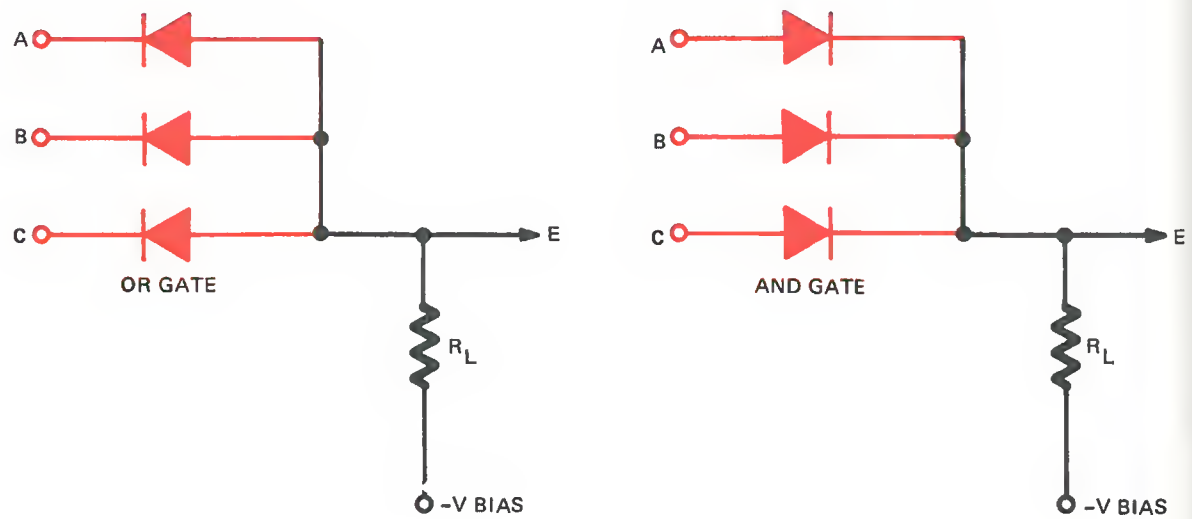


Fig. 9-1 Diode AND and Diode OR Gates (For Negative Logic)

than the applied negative bias voltage at the lower end of the load in figure 9-1. The truth table for the OR gate is shown in figure 9-2.

INPUT			
A	B	C	OUTPUT
0	0	0	0
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	1
0	1	1	1
1	0	1	1
1	1	1	1

Fig. 9-2 Truth Table for an OR Gate

In summary, the OR circuit says, "You get an output if there is an input at A, or B, or C, or · · · N."

The AND circuit, on the other hand, requires that an input be present at A and B and C and · · · N in order to obtain an output. The Boolean equation for the AND gate circuit is

$$ABC = \text{Output} \qquad (9.2)$$

The truth table for an AND circuit is shown in figure 9-3.

INPUT			
A	B	C	OUTPUT
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

Fig. 9-3 Truth Table for an AND Circuit

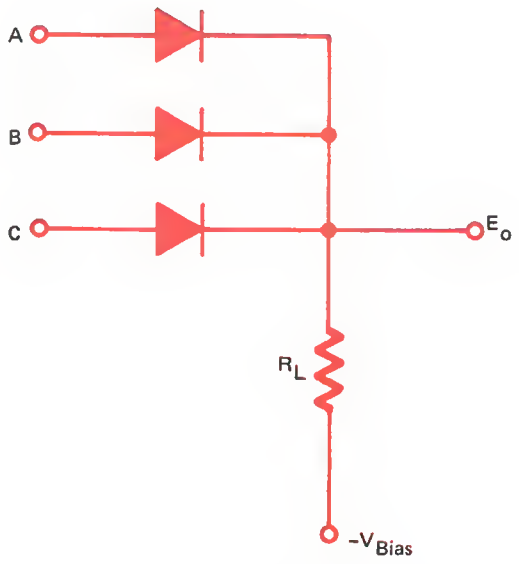


Fig. 9-4 An OR Circuit for Positive Going Pulses

In the case of the OR circuit, the electronics is almost trivial. Pulses which appear at the input are accepted or rejected according to their polarity. Reversing the diode will select pulses of the opposite polarity. Figure 9-4 shows an OR gate for positive pulses. As long as the R_L is many times larger than the forward drop of the diode, the output voltage will approximately equal the input voltage (with a slight loss due to the forward resistance of the diodes). Due to the losses across the diodes, it is not usually practical to use extremely long strings of diode gates in series without reestablishing the signal level occasionally.

AND circuit electronics may require somewhat more extensive examination. Because of the bias voltage at R_L, all the diodes are conducting with no input signal. The total voltage of the bias is dropped across R_L or

$$\text{(The voltage drop across } R_L) \; V_{RL} = V_{Bias} \qquad (9.3)$$

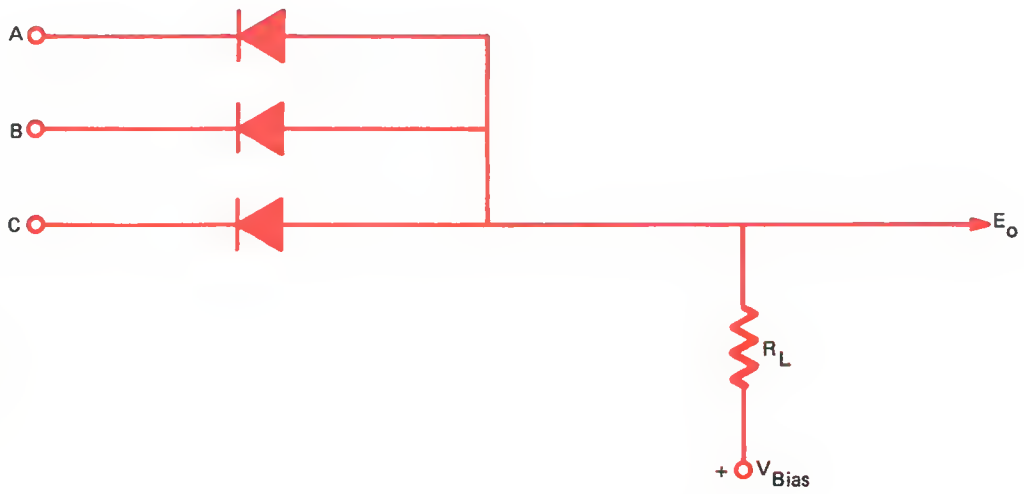


Fig. 9-5 Positive AND Gate

Since all of the supply voltage V_{Bias} is dropped across R_L, no output voltage will appear between the output terminal and ground.

$$E_o = 0V \qquad (9.4)$$

Figure 9-5 shows an AND gate for positive pulses. A gate for negative input pulses can be made by reversing the diodes *and* the polarity of the voltage to R_L. In figure 9-5, when pulses of the correct polarity (+) and magnitude (equal to V_{Bias}) appear at an input, the diode at that input stops conducting. However, the remaining diodes are still conducting and the V_{Bias} will still be entirely dropped across R_L. Consequently we will still have zero volts at the output point. If inappropriate pulses appear at any of the inputs, one or more of the diodes may be turned off; but the remaining diodes will conduct and continue to drop all the bias voltage across R_L. The only time there will be an output will be when all the diodes receive the proper pulses and are turned off. At that time, the R_L voltage drop goes to zero, and the bias voltage (or supply voltage) appears at the output.

These are the most basic and perhaps most important of the gate circuits. The symbols used in logic schematics and reference works are shown in figure 9-6 for the AND gate and in figure 9-7 for the OR gate.

Many other logic gates are used in practical logic circuits. Resistor-capacitor gates are used as are many types of transistor

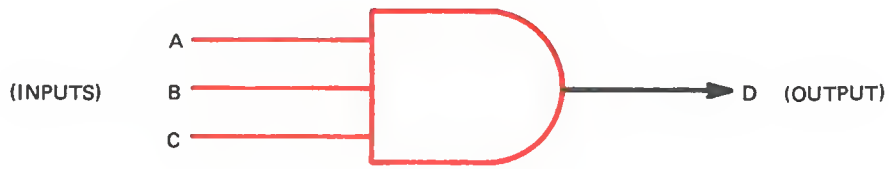


Fig. 9-6 Three Input AND Gate Symbol

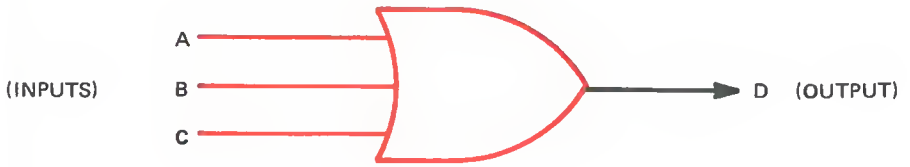


Fig. 9-7 Three Input OR Gate Symbol

gates. The transistor gates have the important advantage of being able to provide amplification to the output. This is particularly important when long strings of series gates are employed.

A particularly interesting diode gate, the diode inhibitor, is shown in figure 9-8. This is a sort of backward AND gate that has a zero output when all the pulses are present. Its truth table would be the reverse of a normal AND gate. With no input at A or B and only the inhibitor signal at C, the A and B diodes will conduct, provided the inhibitor voltage is sufficient to hold diode C cut off.

$$-V_1 + V_{RL} = 0 \qquad (9.5)$$

In this case, $-V_1$ is the bias applied to R_L while V_{RL} is the voltage drop across the load resistor. With A and B conducting, the clamp diode will also be conducting, and the output will be clamped to the V_2 voltage.

In the case of a negative input pulse to A, it would stop conducting but B would still conduct and the output would remain clamped to V_2. The same thing happens with a negative input pulse at B. When negative pulses are applied at *both A and B,* the diodes are both cut off, but the output goes to $-V_1$ because the voltage drop across $R_L = 0$. Inhibition will occur when a positive pulse with a magnitude at least equal to V_1 is applied to C and at the same time A and B receive negative pulses. A and B will be cut off but C will be forced into conduction by the positive pulse, a current will flow through the load and E_o will not change level.

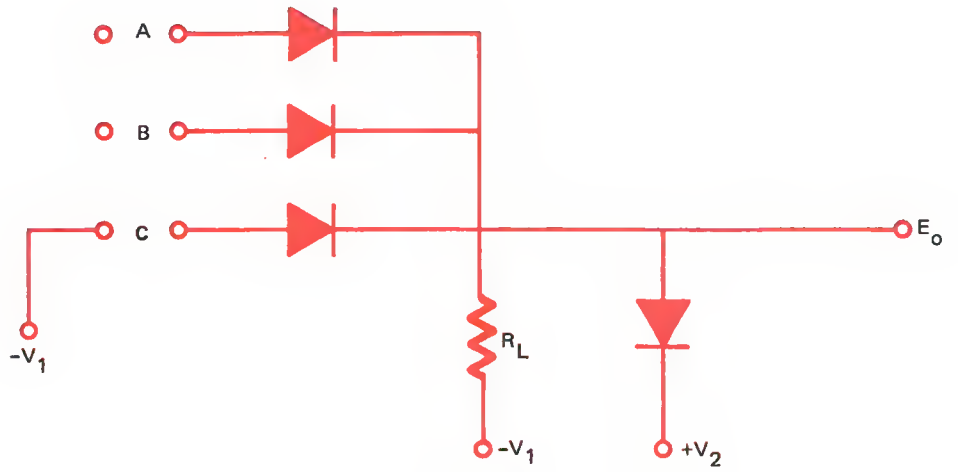


Fig. 9-8 Inhibitor Gate

MATERIALS

2 Semiconductor diodes (breakdown potential greater than 5V)
1 DC power supply (0–40V)
1 Oscilloscope
2 Resistance substitution boxes (15Ω – 10 megΩ)
1 Function generator

PROCEDURE

1. Connect the circuit shown in figure 9-9.

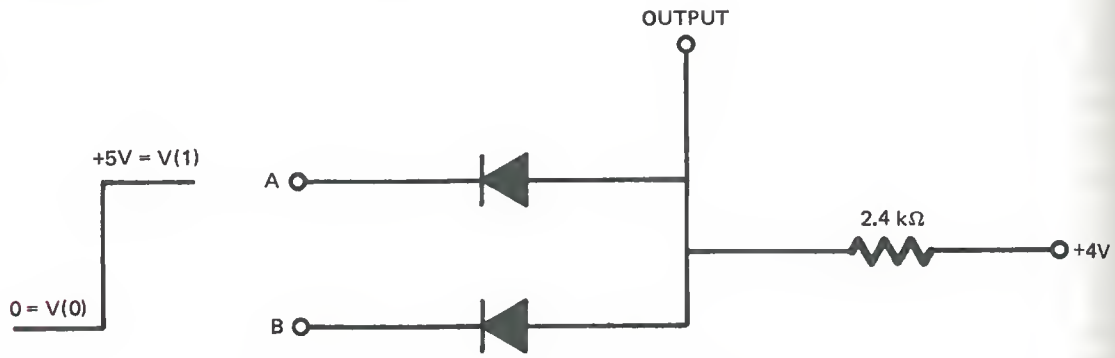


Fig. 9-9 The First Experimental Circuit

2. Apply approximately +5 volt pulses at 1 kHz to input A. Measure and record the output. (Leave B input at zero volts.)
3. Apply approximately +5 volt pulses at 1 kHz to input B while A is at zero volts. Measure and record the output waveform.
4. Apply +5 volt pulses at 1 kHz to both A and B. Measure and record the output waveform. Record the type of gate. (positive Logic)
5. Disassemble the circuit, and assemble the circuit in figure 9-10.

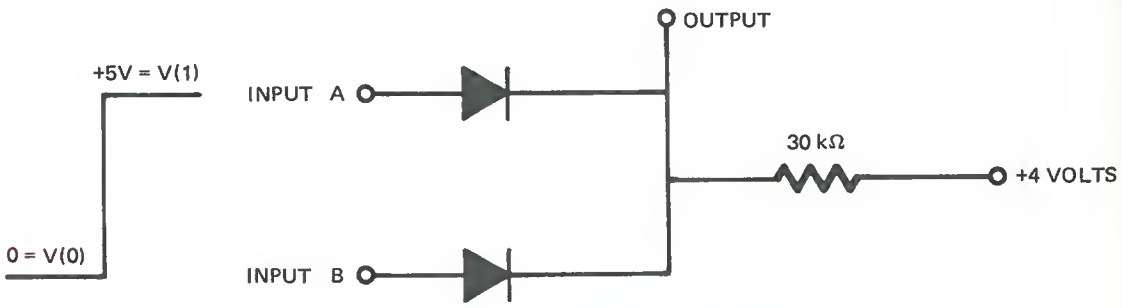


Fig. 9-10 The Second Experimental Circuit

6. Apply +5 volt, 1 kHz pulses at A with B at zero volts. Measure and record the output waveform.

7. Apply +5 volt, 1 kHz pulses at B with A at zero volts. Measure and record the output waveform.
8. Apply +5 volts, 1 kHz pulses at A and B. Measure and record the output waveform and type of gate. (Positive Logic)
9. Disassemble the circuit and build a two input gate that will accept negative pulses of +3V at 1 kHz.
10. Construct a truth table for your circuit, and give its Boolean equation.

ANALYSIS GUIDE. In this experiment the diode as a gate device has been examined. In analyzing these results, an explanation of the diode action should be given. Also discuss the operation of each of the experimental gates using your waveforms to illustrate their operation.

Input	Output
A = +5	
B = 0	

Output Waveform

Input	Output
A = 0	
B = +5	

Output Waveform

Fig. 9-11 The Data Tables

Input	Output										
A = +5											
B = +5											
Circuit Type											

Output Waveform

Input	Output										
A = +5											
B = 0											

Output Waveform

Input	Output										
A = 0											
B = +3											

Output Waveform

Fig. 9-11 The Data Tables (Cont.)

Input	Output										
A = +3											
B = +3											
Circuit Type											

Output Waveform

Circuit Diagram for Two Input and Gate

Fig. 9-11 The Data Tables (Cont.)

INPUTS		
A	B	OUTPUT

BOOLEAN EQUATION

Fig. 9-11 The Data Tables (Cont.)

PROBLEMS

1. Given a load resistor to ground from a diode AND gate, R_L = 5.1 kΩ and two inputs at the diodes of 0 and +2 volts DC. What will the output level be?
2. Will AND gates have slightly higher or slightly lower output levels if silicon diodes are used in place of germanium? Why?
3. In the circuit of figure 9-10, what will be the effect of an open diode at A?

INTRODUCTION. Basic logic operations may be performed by either diodes or transistors. In this experiment we shall examine transistorized logic gates of perhaps the simplest type. These gates are constructed using only resistors and transistors. They are often referred to as RTL circuits.

DISCUSSION. Let's consider the operation of the circuit shown in figure 10-1. The transistor Q_1 is biased to cutoff by the base supply V_{BB}. If we apply a sufficiently negative pulse to any one of the inputs, then the transistor can be turned on. If a single input pulse drives the transistor completely into saturation, then applying another pulse to another input will only drive the transistor further into saturation if that is possible. As a result, the circuit acts like an *OR* gate. However, since driving the base negative causes the collector to go positive, the output is inverted. Such an *inverted/OR* gate is often called a *negative OR* gate or, more simply, a *NOR* gate. The Boolean expression for such a gate is

$$A + B + C = -E_o \qquad (10.1)$$

where E_o is the output and the negative sign indicates the polarity reversal across the gate.

Appropriate values for the various circuit resistances can be readily determined using the transistor input and output characteristics. For example, let's consider the curves shown in figure 10-2.

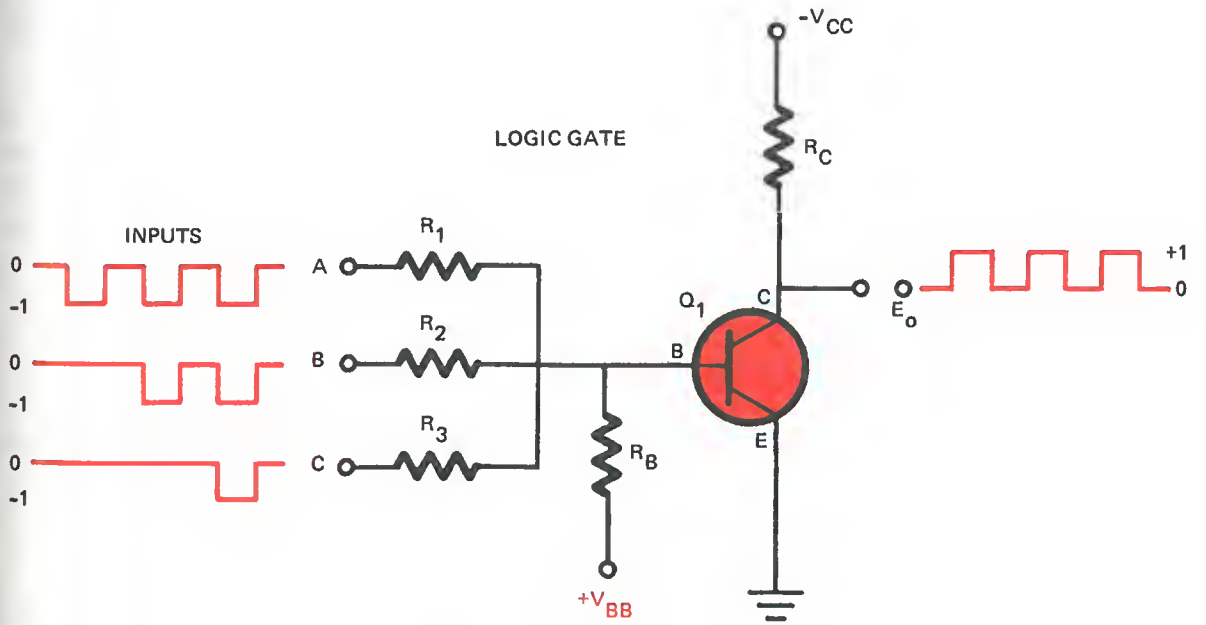


Fig. 10-1 An Inversion/OR (NOR) Gate

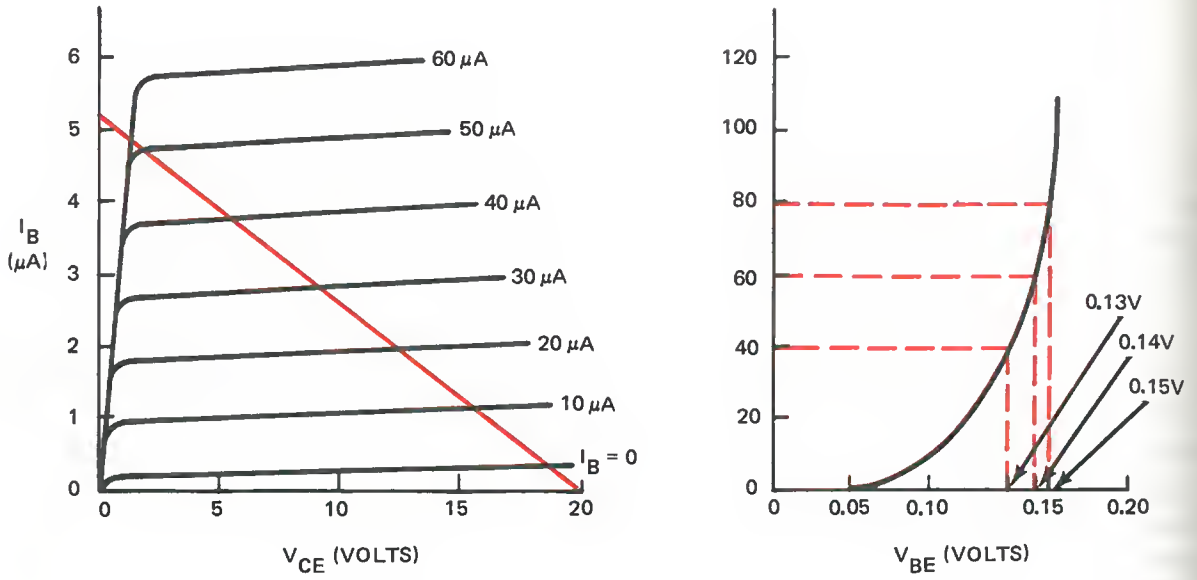


Fig. 10-2 Transistor Characteristics

Suppose the collector supply (V_{CC}) is to be -20 volts and V_{BB} is +10 volts. To choose R_C we first choose some reasonable maximum collector current ($I_{C\ SAT}$). From the output curve (V_{CE} vs I_C) we see that about 5 mA would be reasonable. The collector resistor would then be

$$R_C = \frac{V_{CC}}{I_{C\ SAT}} = \frac{20}{5\ mA} = 4\ k\Omega$$

Since this is not a standard size, we would probably use 3.9 kΩ, which is the nearest standard size. Then we would plot the collector load line from V_{CC} to

$$I_{C\ max} = \frac{V_{CC}}{R_C} = \frac{20}{3.9k} \cong 5.1\ mA$$

With the load line plotted we observe that a base current of 60 μA or more is required for saturation. ($I_{B\ SAT} = 60\ \mu A$)

Using this value ($I_{B\ SAT} = 60\ \mu A$) with the input characteristic, we observe two things. First, $V_{BE\ on}$ will be approximately 0.15 volts. And second, the transistor input resistance is approximately

$$R_{in} \cong \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.15V - 0.13V}{80\ \mu A - 40\ \mu A} = \frac{0.02V}{40\ \mu A} = 500\Omega$$

The base resistor R_B is usually chosen to be large enough so that it will not seriously reduce the transistor input resistance. On the other hand, it must not be so large that the transistor will not completely cut off. A value of

$$R_B = 10\ R_{in}$$

is usually quite satisfactory. In our example, this would be

$$R_B = 10\ R_{in} = 5\ k\Omega$$

and we would probably decide to use a 4.7 kΩ resistor.

The input resistors (R_1, R_2, R_3) are usually all equal values

$$R_1 = R_2 = R_3$$

and are chosen to assure that sufficient $I_{B\ SAT}$ will flow when an input pulse is applied, if the input pulses have a height of

$$V_A = V_B = V_C = 10 \text{ volts}$$

To turn the transistor fully on, we must satisfy the relationship

$$R_1 = \frac{V_A - V_{BE\ on}}{I_{B\ SAT}}$$

Therefore, in our example, we have

$$R_1 = \frac{10 - 0.15}{60\ \mu A} = 164\ k\Omega$$

Since this is not a standard size, we would normally use the next smaller standard size. Using a smaller size assures us of having more than enough base current. In most practical cases, $V_{BE\ on}$ is so small compared to the input pulse height that we can use simply

$$R_1 = \frac{V_A}{I_{B\ SAT}}$$

which would give 167 kΩ in our example. In either case, we would probably use 150 kΩ for the input resistors.

The RTL circuit shown in figure 10-1 is perhaps one of the most versatile logic circuits available.

If we merely change the value of R_B to a value which will hold the circuit cut off if *all but one* input is applied, and saturate it when *all* inputs are applied, then we have an inverted AND gate. Such a gate is called a NAND gate.

The equivalent circuits of the two input conditions are shown in figure 10-3 for N inputs.

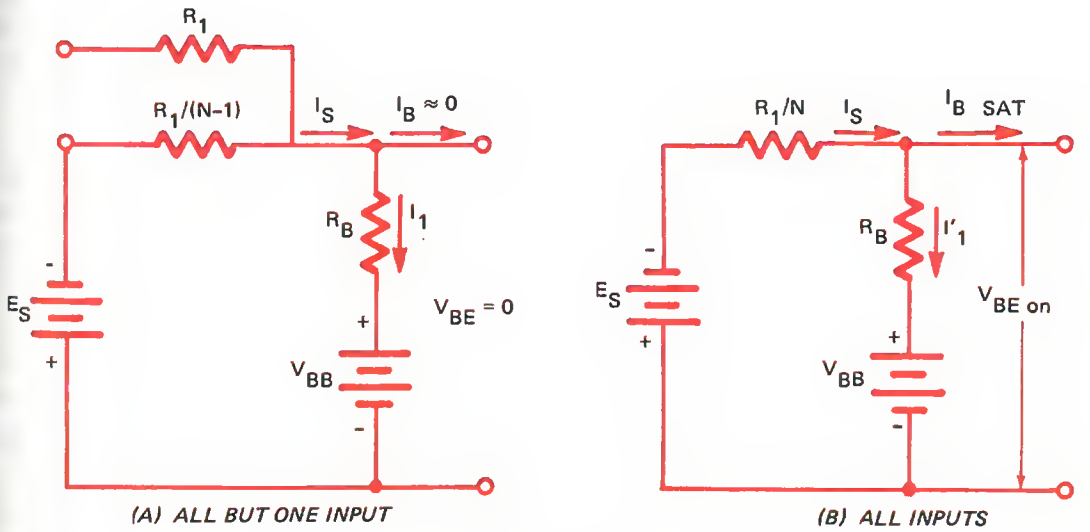


Fig. 10-3 Input Conditions for a NAND Gate (with N inputs)

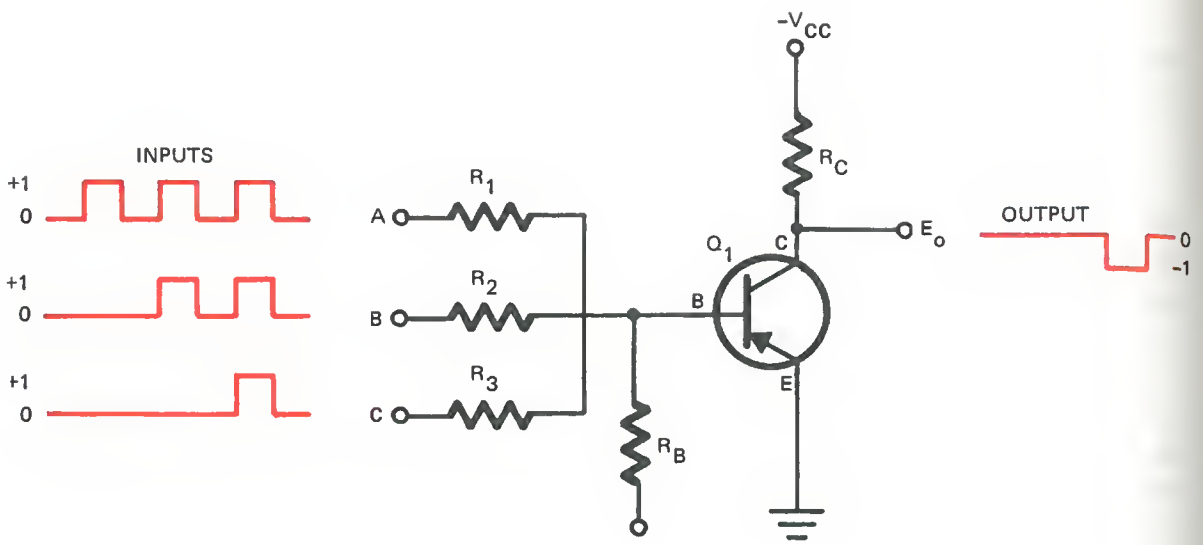


Fig. 10-4 An Inversion/AND (NAND) Gate

The two equations which describe these circuits are

$$I_S - I_1 = 0 \text{ and } I_S - I'_1 = I_{B\ SAT}$$

Assuming that E_S and V_{BB} are both much greater than $V_{BE\ on}$, we can reduce these conditions to circuit values of

$$R_B = \frac{V_{BB}}{(N-1)\ I_{B\ SAT}} \text{ and } R_1 = \frac{E_S}{I_{B\ SAT}}$$

Hence, the Boolean equation becomes

$$ABC = -E_o \qquad (10.2)$$

where the minus sign indicates inversion.

If we *reverse the polarity of the base* (V_{BB}) *supply,* the circuit will appear as shown in figure 10-4. In this case, the transistor Q_1 is forward biased deep into saturation with no inputs present. If we apply a single positive input pulse (A), the circuit will not cut off because it is too deeply saturated. If we apply two inputs (A and B), the circuit will not cut off but will now be only slightly saturated. But if we apply all three positive inputs at the same time (A and B and C), then the circuit will cut off. When this happens, we get a single negative output pulse. We can say, therefore, that the circuit acts as an inverting AND or a NAND gate.

Choosing the circuit resistances is somewhat more involved than for a NOR gate. However, R_C can be selected the same way as before.

The base resistor must be chosen such as to provide sufficient saturation current that only the final input pulse will switch the transistor from saturation to cutoff.

We must, therefore, satisfy two conditions simultaneously. First, when all but one input is applied, then the transistor must still be saturated. That is, V_{BE} must still be greater than $V_{BE\ on}$ and I_B must exceed $I_{B\ SAT}$. Secondly, when all inputs are present, the transistor must be cut off. That

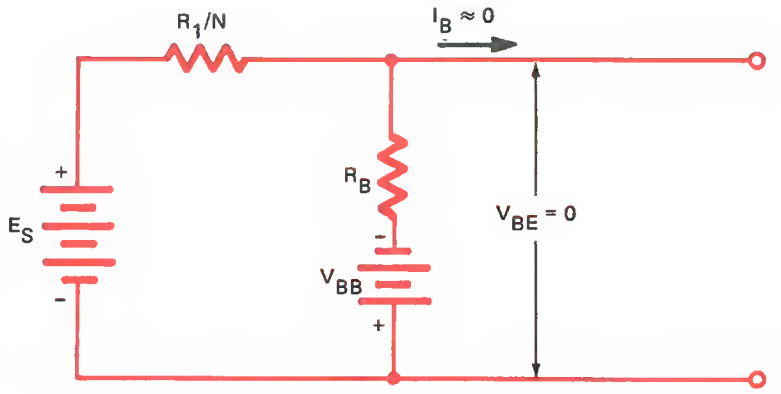


Fig. 10-5 Equivalent Circuit at Cutoff

is, V_{BE} must be approximately zero (or perhaps even a little reverse biased), and I_B must also approximate zero. Let's suppose that we choose to have V_{BE} equal to zero at cutoff. We can then draw the equivalent circuit shown in figure 10-5 (assuming $R_1 = R_2 = R_3 = \ldots = R_N$).

From this circuit we see that

$$\frac{V_{BB}}{R_B} = \frac{NE_S}{R_1} \text{ if } I_B = 0$$

where E_S is the height of the input pulses. Similarly, the equivalent circuit for all but one input applied is shown in figure 10-6. From this circuit we have the equation

$$I_{BB} - I_S = I_{B\,SAT}$$

or

$$\frac{V_{BB} - V_{BE\,on}}{R_B} - \frac{E_S + V_{BE\,on}}{R_1}(N-1) = I_{B\,SAT}$$

Solving this equation and the one from figure 10-5 simultaneously and assuming $V_{BB} >>$

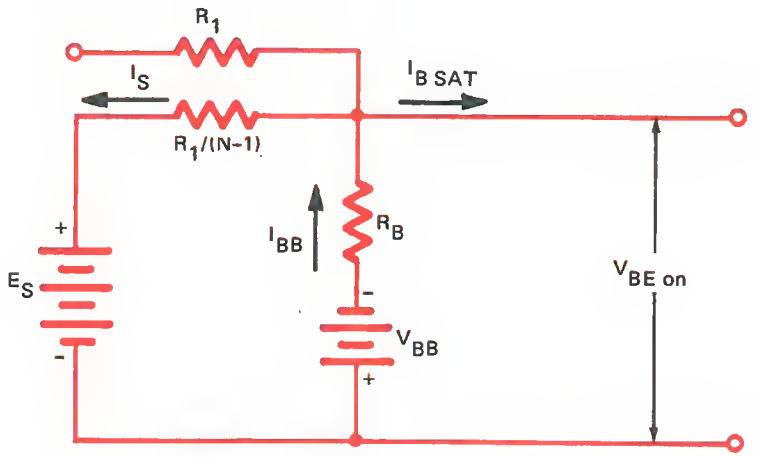


Fig. 10-6 Equivalent Circuit with (N-1) Inputs

$V_{BE\ on}$ AND $E_S >> V_{BE\ on}$ gives us

$$R_B \cong \frac{V_{BB}}{I_{B\ SAT}} (1/N)$$

and

$$R_1 \cong \frac{E_S}{I_{B\ SAT}}$$

Using the values from our previous example, these equations render

$$R_B \cong 55.5\ k\Omega$$

and

$$R_1 = R_2 = R_3 = 166\ k\Omega$$

In this case, we would probably use values of 56 kΩ and 168 kΩ respectively.

As was the case before we can change the logic function by selecting another set of circuit component values. If R_B is such that the circuit is barely saturated with no input, then applying any one input can cut it off. This set of conditions would give us circuit values of

$$R_B = \frac{V_{BB}}{I_{B\ SAT}} \text{ and } R_1 = \frac{E_S}{I_{B\ SAT}}$$

And the Boolean expression becomes

$$A + B + C = -E_o$$

Or, in other words, the circuit performs the NOR operation.

Using NAND and NOR gates rather than AND and OR, usually do not present any serious problems since the output of a gate can always be INVERTED if necessary. Figure 10-7 shows a typical logic inverter. By coupling this circuit to the output of a NAND or NOR gate, we can convert to AND and OR logic.

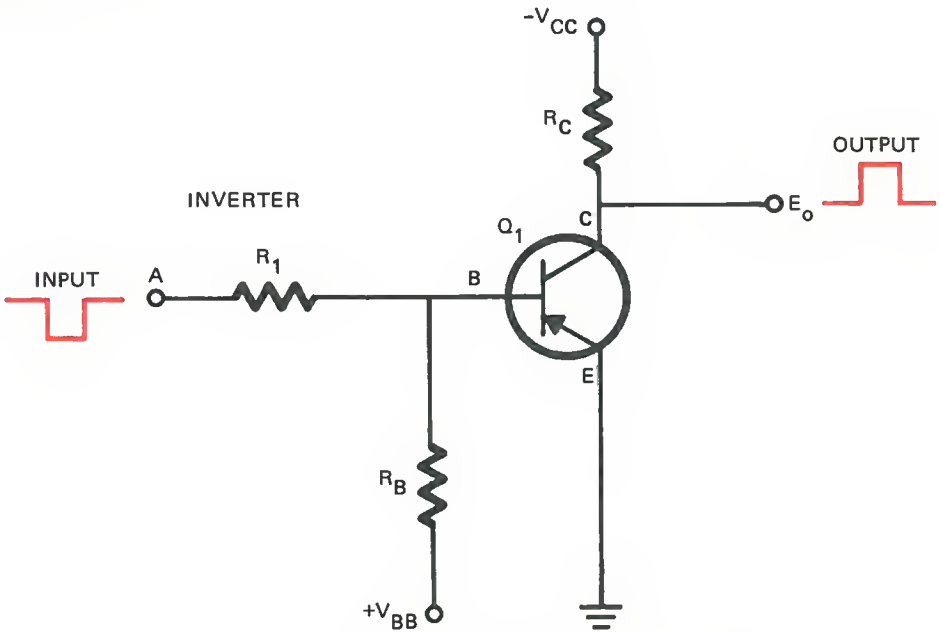


Fig. 10-7 A Logic Inverter

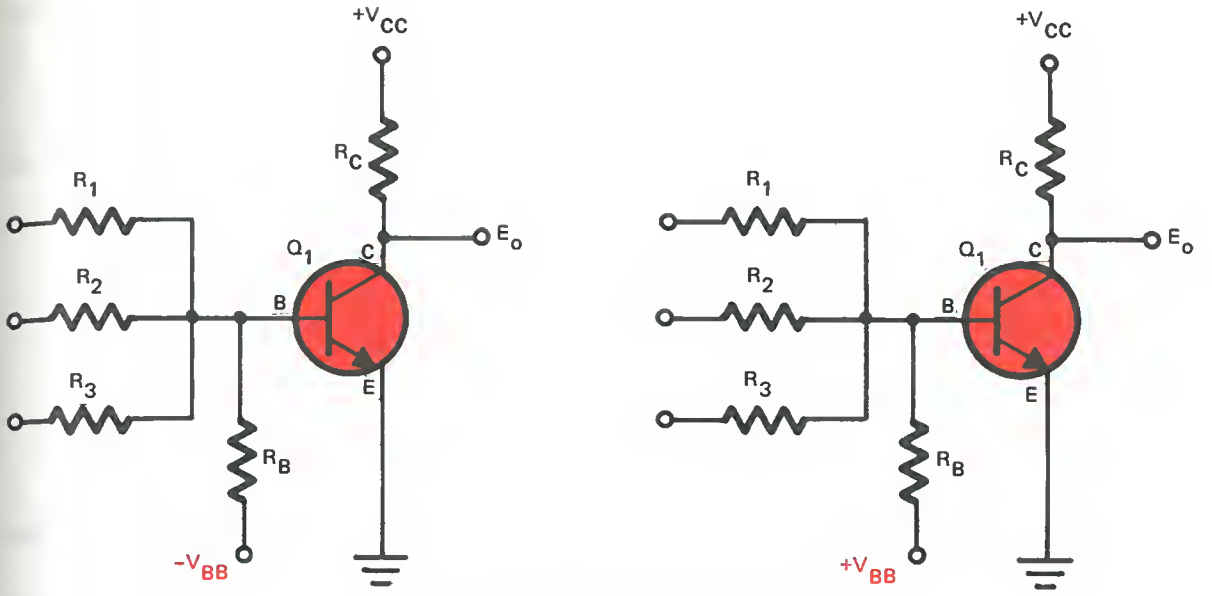


Fig. 10-8 NPN Logic Gates

In an inverter R_C is chosen as before, $R_1 = R_B = 10\ R_{in}$ provides satisfactory values for the input circuit.

The logic gates discussed up to this point have used PNP transistors only. Similar circuits can, of course, be constructed using NPN transistors. Figure 10-8 shows a NAND and a NOR gate employing NPN devices You should be able to figure out which is the NAND and NOR gate by yourself.

MATERIALS

- 2 DC power supplies (0-40V)
- 1 VOM or FEM
- 2 Transistors, type 2N1304 and 2N1305 or equivalent
- 1 Set of curves for the transistors
- 8 Resistors (values to be determined by student)
- 1 Breadboard
- 2 Transistor sockets

PROCEDURE

1. Examine your two transistors and decide which one you will use for a logic gate.
2. Using your transistor curves, determine an appropriate value of collector resistor to use with $V_{CC} = 10$ volts.
3. Determine the appropriate values to use for R_B, R_1 and R_2, with a two input NAND gate which has a V_{BB} of 10 volts and a E_S of 10 volts. Use the type of circuit shown in figure 10-4.
4. Assemble the appropriate NAND gate circuit using either figure 10-4 or 10-8 as a guide.
5. When your circuit is assembled, measure and record your value of V_{CE} with no input present. Record the polarity too.

6. Connect input A only to a 10-volt potential of the proper polarity. (B input should be grounded.)
7. Measure and record V_{CE} and its polarity.
8. Connect input B only to a 10-volt potential of the proper polarity. (A should be grounded.)
9. Record the value of V_{CE} and its polarity.
10. Connect both input A and input B to a 10-volt potential of the proper polarity.
11. Record the value of V_{CE} and its polarity.
12. Prepare a truth table of your observations from steps 5 through 11.
13. Reverse the polarity of V_{BB}, then repeat steps 5 through 12.
14. Compute the values of R_C, R_B, and R_1 that you would use for an inverter of the type shown in figure 10-6.
15. Using your remaining transistor, construct an inverter and connect it to the output of your logic gate circuit.
16. Repeat steps 5 through 12 again and this time measure the V_{CE} of the inverter stage.
17. Again reverse the polarity of V_{BB} and repeat steps 5 through 13, recording the V_{CE} of the inverter stage.
18. Draw a complete circuit diagram of each of the setups used, showing circuit values, transistor type, and power supply polarities.

ANALYSIS GUIDE. In analyzing the data from this experiment, you should discuss each circuit used and the results observed. Give the Boolean equation which describes each circuit and tell what it means. Also discuss how your truth tables verify each Boolean equation.

Discuss how you can tell if an RTL circuit is a NAND or a NOR gate.

	V_{CE} No Input	V_{CE} Input A Only	V_{CE} Input B Only	V_{CE} Input A & B
First Circuit				
Second Circuit				
Third Circuit				
Fourth Circuit				

Measured Data

Fig. 10-9 The Data Table

Circuit Diagram

Fig. 10-9 The Data Table (Cont.)

PROBLEMS

1. Using the methods outlined in the discussion, compute the component values for the circuit shown in figure 10-10.

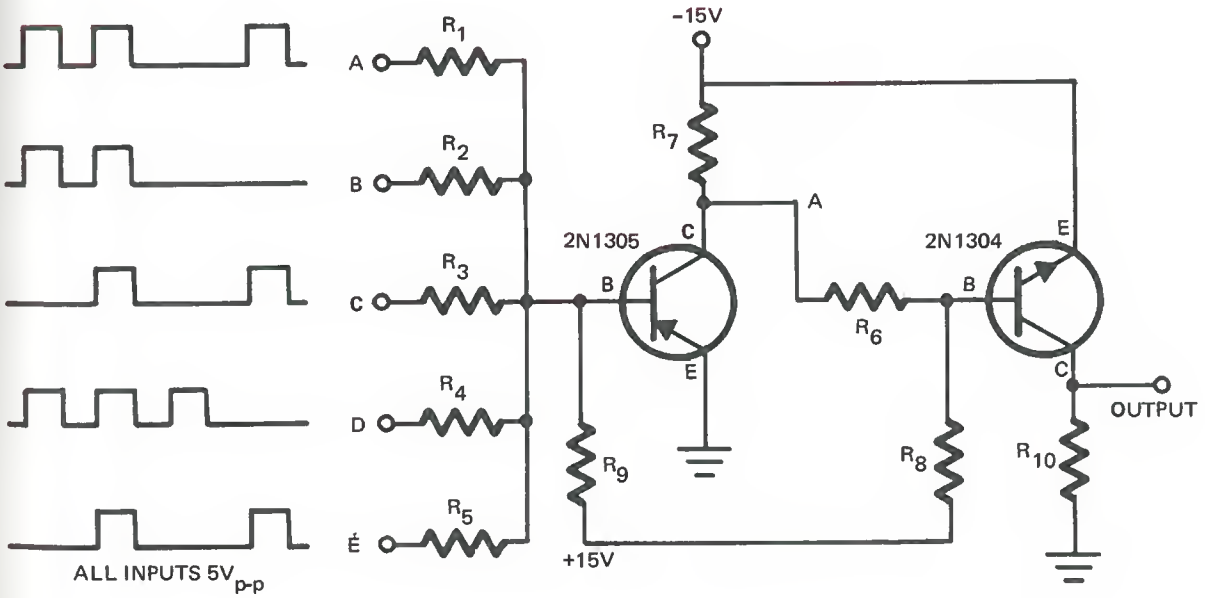


Fig. 10-10 Circuit for Problem 1

2. Make a sketch of the input and output waveforms for the circuits in figure 10-8.
3. What would be the peak-to-peak signal voltage at the output of the circuit in figure 10-10?
4. What is the Boolean equation for the circuit in figure 10-10?
5. Explain in your own words how the inverter in figure 10-10 works.

INTRODUCTION. There are a variety of *direct-coupled* transistor circuits which are used to perform logic operations. In this experiment we will examine some of the more common direct-coupled transistor logic (DCTL) circuits.

DISCUSSION. Let's look at the circuit given in figure 11-1. Suppose that the steady state currents supplied to the three input bases are zero. All three transistors will, therefore, be cut off. If a negative pulse is applied to input A only, the transistor Q_1 would want to turn on. However, since both Q_2 and Q_3 are cut off, no current can flow through R_C and the output voltage would be equal to $-V_{CC}$.

If pulses are applied simultaneously to inputs A and B, both Q_1 and Q_2 would want to come on. However, since Q_3 is still cut off the output would remain at $-V_{CC}$.

If we apply simultaneous pulses to all three inputs, then all three transistors will come on and current will flow through R_C. The output voltage will rise to approximately zero.

The overall result, then, is that we will get an output pulse only when we apply negative inputs to all three bases simultaneously. This circuit then is a NAND gate and provides the Boolean operation,

$$ABC = -E_o \qquad (11.1)$$

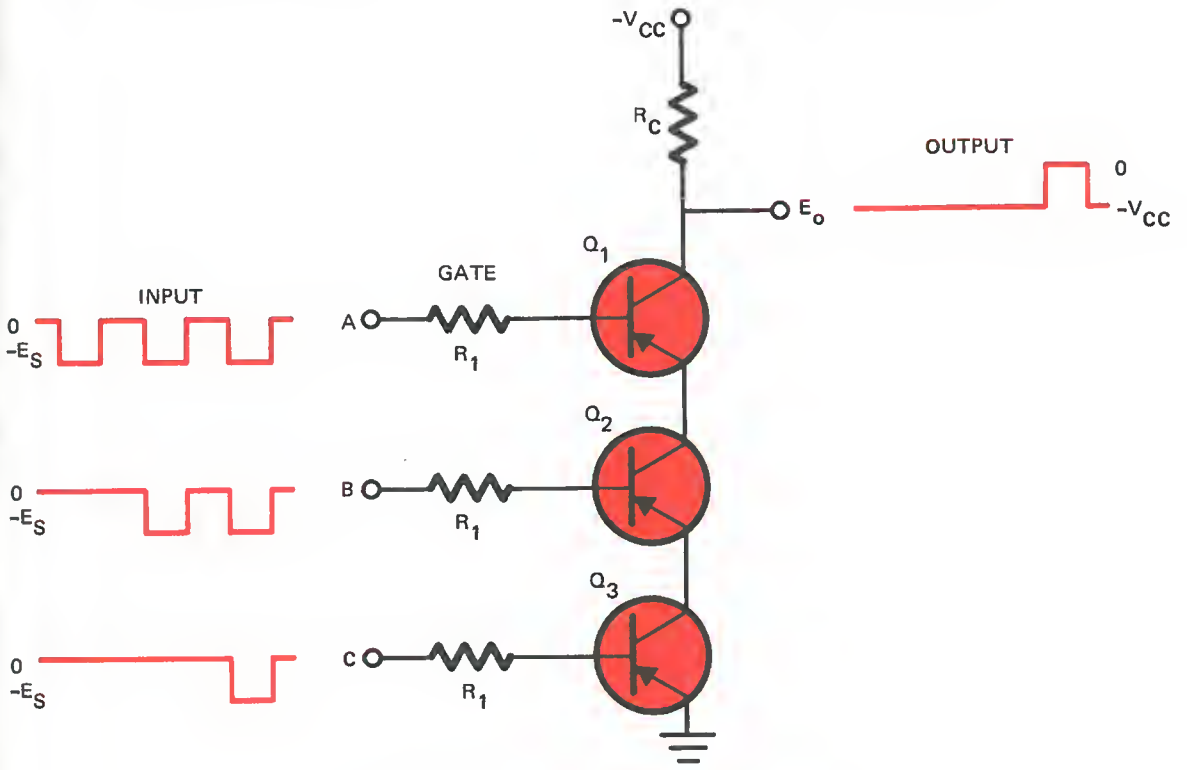


Fig. 11-1 A Series DCTL NAND Gate

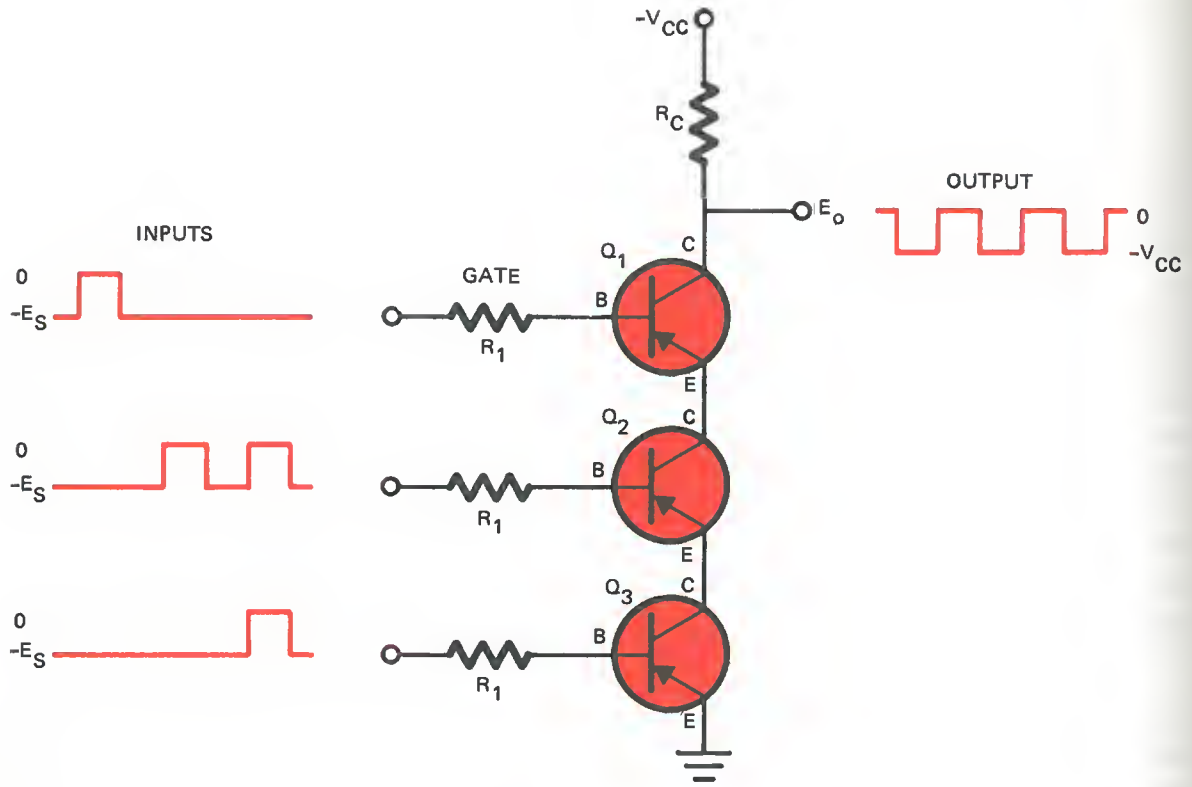


Fig. 11-2 A Series DCTL NOR Gate

The DCTL circuit shown in figure 11-1 has a logical dual as you might expect. The dual of the series DCTL is shown in figure 11-2.

Suppose that all three inputs are connected to other logic circuits which normally cut off producing signals which are at a negative voltage. (Figure 11-1 was such a circuit.)

In such a case the transistor Q_1, Q_2, and Q_3 are normally on and the output of the gate is normally near zero. If any one of the transistors receives a positive pulse it cuts off and the output drops to $-V_{CC}$. The circuit is, therefore, a NOR gate and its Boolean expression is

$$A + B + C = -E_o \qquad (11.2)$$

Series DCTL circuits can, of course, be constructed with either NPN or PNP transistors, the only difference being the polarity of V_{CC}, and of the input signals.

In building series DCTLs, only the value of R_C need be determined. This can be done by choosing a safe value of $I_{C\ max}$ and computing R_C.

$$R_C = \frac{V_{CC}}{I_{C\ max}} \qquad (11.3)$$

Some applications require that the transistors be biased individually. Figure 11-3 shows a typical bias arrangement.

Such a circuit may be either a NAND or NOR gate, depending on the polarity of the bias. By now you should be able to determine which type of gate would result from each bias polarity.

DCTL circuits can also be made using parallel transistors. Figure 11-4 shows one

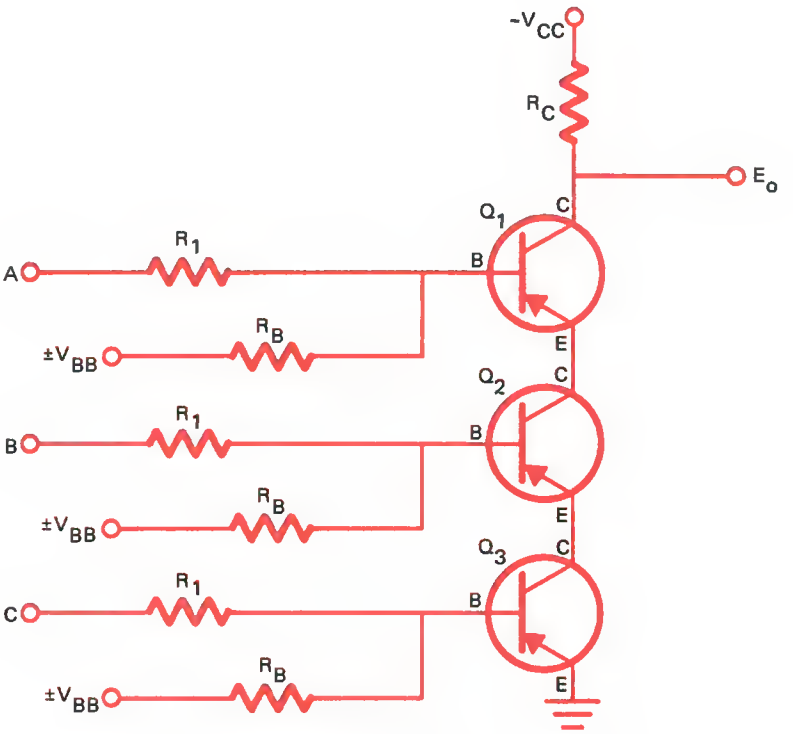


Fig. 11-3 Separatelv Biasing a Series Gate

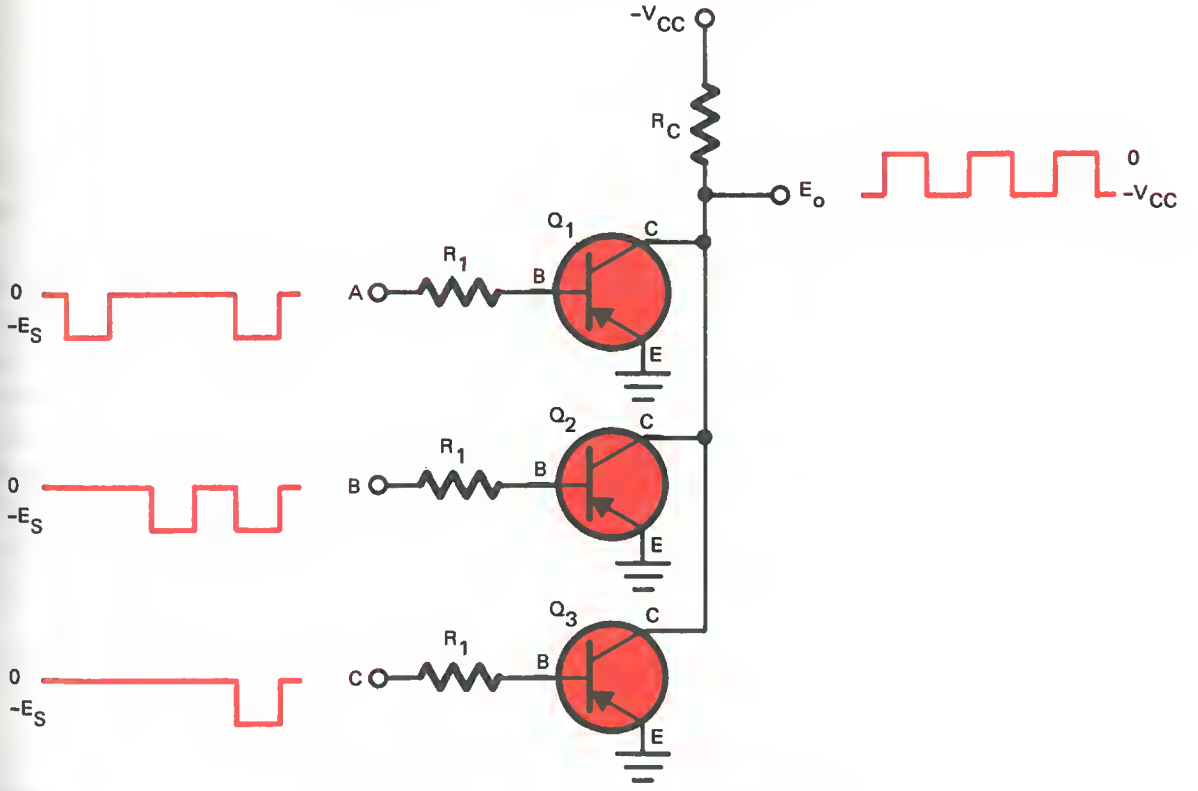


Fig. 11-4 A Parallel DCTL NOR Gate

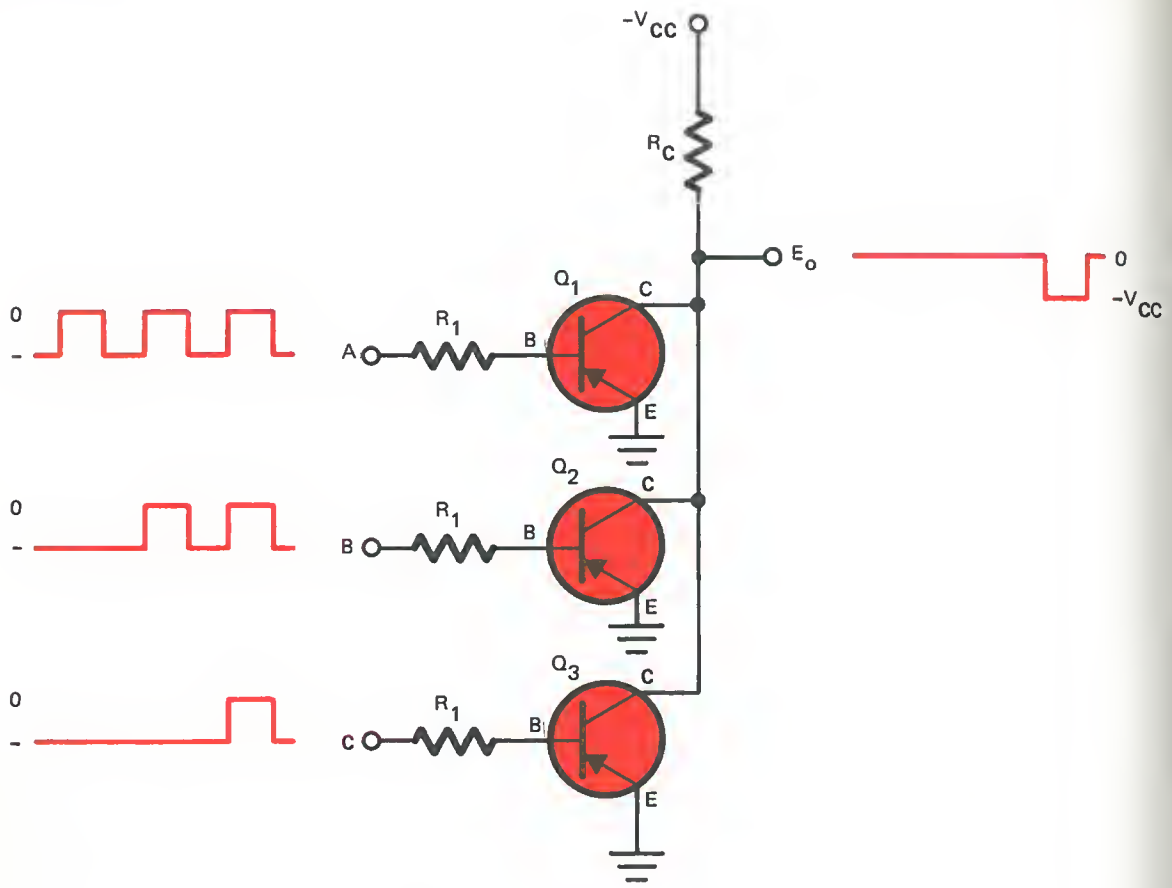


Fig. 11-5 A DCTL NAND Gate

such circuit. In this circuit all three transistors are normally cutoff and the output voltage is normally at $-V_{cc}$.

If a negative input pulse is applied to any one of the transistors, it turns on and the output rises to near zero. The gate is therefore, of the NOR type and has

$$A + B + C = -E_o \qquad (11.4)$$

for its Boolean expression.

If the inputs are connected to sources which normally have a negative level and produce positive signal pulses we have the logic dual of the parallel DCTL circuit. Figure 11-5 shows the parallel dual case.

In this circuit all three transistors are normally on and the output level is normally near zero. If we turn off one of the transistors, the output stays near zero because the other two transistors are still on. Similarly, if we turn off two of the transistors, the output is still near zero due to the conduction of the last transistor. But if we turn off all three transistors the output falls to $-V_{CC}$.

We can see, therefore, that the circuit acts as a NAND gate. The Boolean expression is consequently

$$ABC = -E_o \qquad (11.5)$$

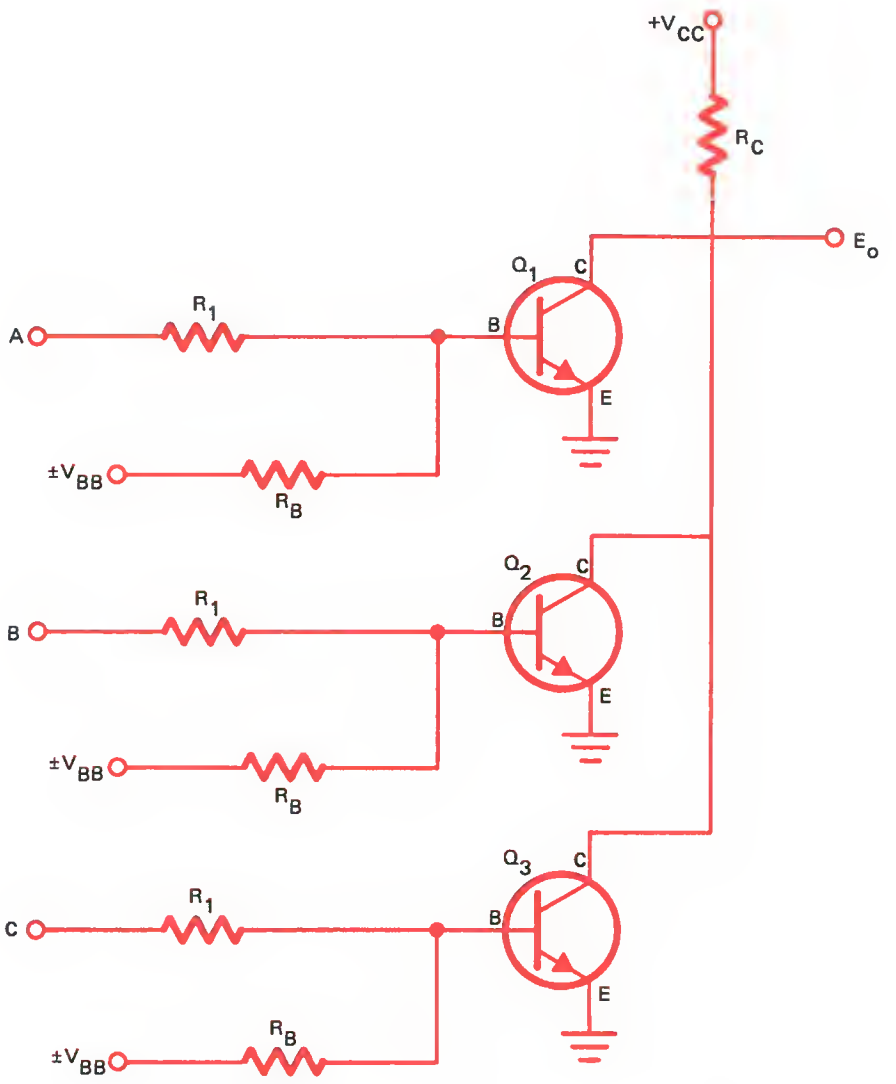


Fig. 11-6 A Separately-Biased Parallel Gate

As was the case with series DCTL circuits, we need only find the value of R_C to build a parallel DCTL gate. Also, like the series circuits, we simply choose a safe value of $I_{C\ max}$ and compute

$$R_C = \frac{V_{CC}}{I_{C\ max}}$$

We can use either PNP or NPN transistors to build parallel DCTLs and we can separately bias them if necessary. Figure 11-6 shows a separately biased NPN circuit.

You should know by now which type of gate would have positive bias and which type would have negative bias.

Selecting a base resistor value is almost always done simply by laying out the load line of R_C and determining the value of the saturation base current. R_B is then calculated using

$$R_B = \frac{V_{BB}}{I_{B\ SAT}} \qquad (11.6)$$

This value will normally be satisfactory for either series or parallel NAND or NOR gates.

Similarly, the input resistors are chosen to limit base current to a safe value, say twice $I_{B\ SAT}$.

$$R_1 = \frac{E_S}{2I_{B\ SAT}} \qquad (11.7)$$

MATERIALS

- 3 Transistors type 2N1304 or 2N1305 or equivalent
- 1 Set of output characteristics for the above
- 1 VOM or FEM
- 2 DC power supplies (0–40V)
- 4 Resistors, values to be determined by student
- 1 Breadboard
- 3 Transistor sockets

PROCEDURE

1. Choose a value of R_C which is appropriate for use with your transistor type and a V_{CC} of 10 volts.
2. Compute a value of R_1 which is appropriate for your transistor, R_C, and E_S of 10 volts.
3. Construct a circuit similar to figure 11-1. Measure the output with no input signal.
4. Apply a voltage of correct polarity to input A only and record the output voltage.
5. Repeat step 4 with input B only, then with input C only.
6. Apply the voltage of correct polarity to inputs A and B simultaneously. Record the output voltage.
7. Repeat step 6 using inputs B and C, then A and C.
8. Now apply the signal to all three inputs simultaneously.
9. Prepare a truth table showing the results of steps 3 through 8. Use 0 for no input and zero output. Use 1 for input applied and output = V_{CC}.
10. Write the Boolean expression which represents the results in your truth table.
11. Connect the input signal to all three inputs so that the three transistors are *on*. Record the output voltage.
12. Remove the signal from input A only and record the output voltage.
13. Repeat step 12 with the signal removed from B only, and C only.

14. Disconnect the input signal from A and B simultaneously and record the output.
15. Repeat step 14 for B and C, then A and C.
16. Disconnect the signal from all three inputs and record the results.
17. Prepare a truth table of your results from steps 11 through 16. Use 0 for input connected and output $\cong V_{CC}$. Use 1 for input disconnected and output $\cong$ zero.
18. Write the Boolean expression for your truth table.
19. Construct a circuit similar to figure 11-4 and repeat steps 4 through 18.
20. Draw detailed circuit diagrams for both test circuits showing all circuit values.

ANALYSIS GUIDE. In analyzing your results you should compare the operation of series NAND gates to parallel NAND gates. Explain the operation of each and discuss their similarities and differences. Compare series and parallel NOR gates in the same manner. Which NAND gate do you prefer? Which NOR gate? Why?

First Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts
Boolean Expression				

Fig. 11-7 The Data Tables

Second Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Boolean Expression

Third Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Boolean Expression

Fig. 11-7 The Data Tables (Cont'd)

Fourth Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts
Boolean Expression				

Fig. 11-7 The Data Table (Cont'd)

PROBLEMS

1. Design a series NAND gate using 2N1304s to operate with $|V_{CC}|$ = 15 volts, $|E_S|$ = 5 volts.
2. Repeat problem 1 using a parallel circuit.
3. Repeat problem 1 using a 2N1305.
4. Repeat problem 2 using a 2N1305.
5. Discuss the operation of the circuit shown in figure 11-8. How is it different from figure 11-1?
6. Draw the output waveform for the circuit in figure 11-8.
7. Discuss the operation of the circuit shown in figure 11-9 and sketch the output waveform.
8. Write the Boolean expression for the circuit in figure 11-9.
9. Discuss the operation of the circuit shown in figure 11-10 and sketch the output waveform.
10. Write the Boolean expression for the circuit in figure 11-10.

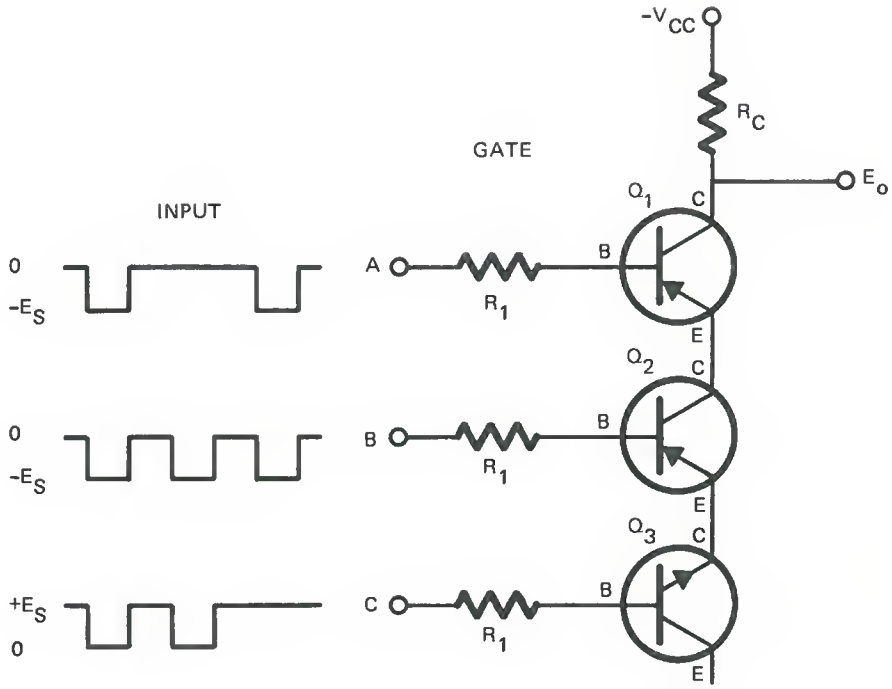


Fig. 11-8 Circuit for Problem Five

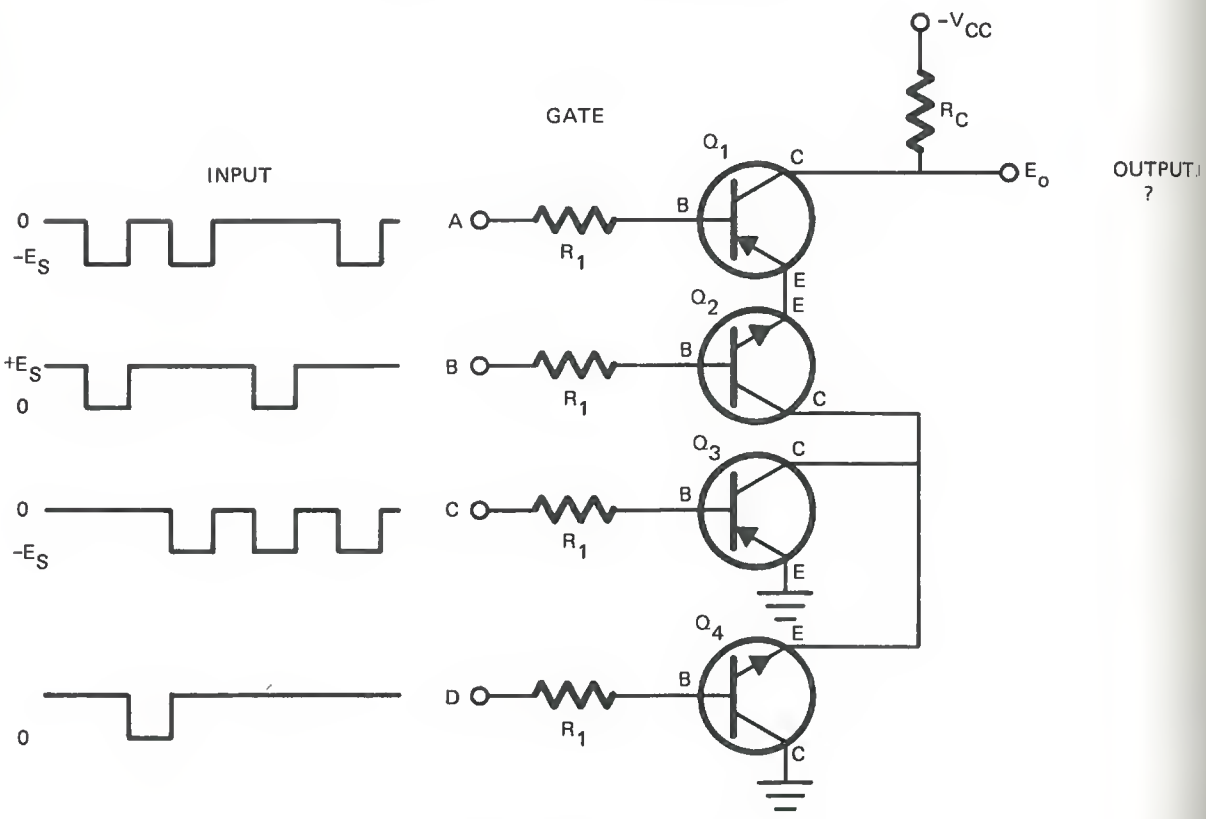


Fig. 11-9 Circuit for Problem Seven

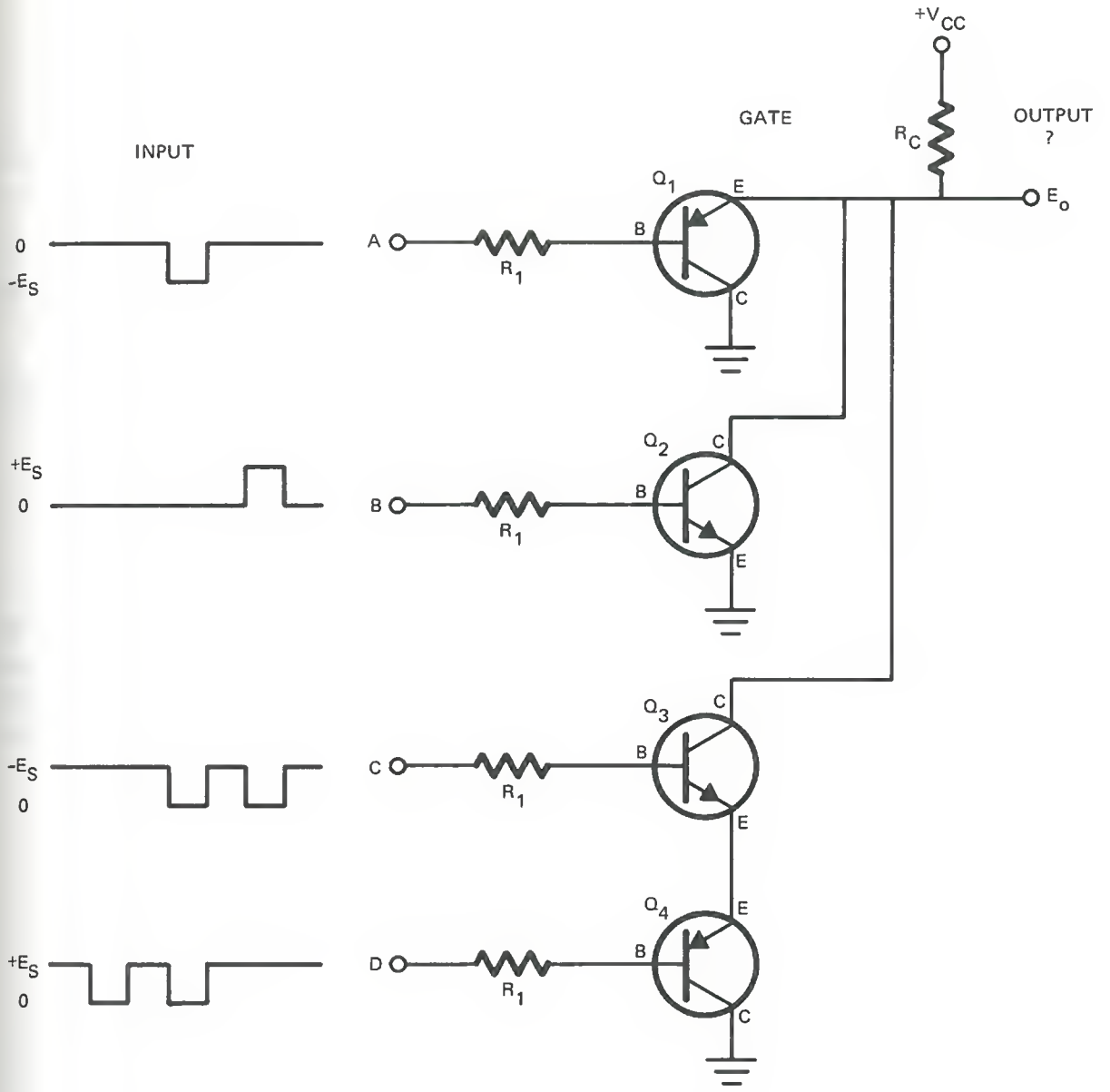


Fig. 11-10 Circuit for Problem Nine

INTRODUCTION. In some logic operations it is necessary to *prevent* a logic gate from operating at certain times. Circuits which prevent logic gate operations are called *inhibitor* circuits. In this experiment we shall examine some of the ways that a logic gate can be inhibited.

DISCUSSION. Let's consider the operation of the series NOR gate shown in figure 12-1.

Inputs A, B, and C are connected to other logic circuits which produce positive pulses from a negative reference voltage. NAND gates could produce this type pulse.

When this arrangement is used, all the transistors are normally on and the output of the gate is at zero volts. When a pulse arrives at the base of any of the transistors, that transistor will be biased to cutoff, and the output will drop to $-V_{CC}$.

The Boolean expression for this series DCTL NOR gate is

$$A + B + C = -E_o \text{ (Inverted Output)} \quad (12.1)$$

The value of R_C can be determined by

$$R_C = \frac{V_{CC}}{I_{C\,max}}$$

where $I_{C\,max}$ is choosen as a safe value for the device. By reversing the polarity of V_{CC} and inverting the output, the circuit in figure 12-1 could be constructed with NPN transistors.

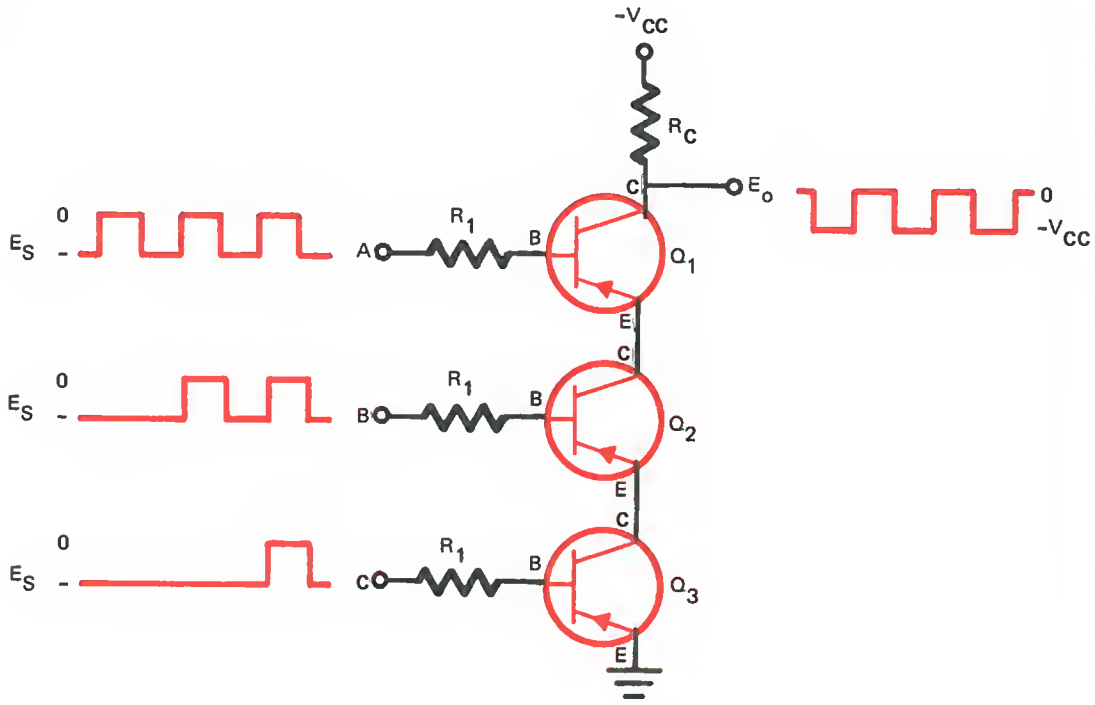


Fig. 12-1 Series NOR Gate

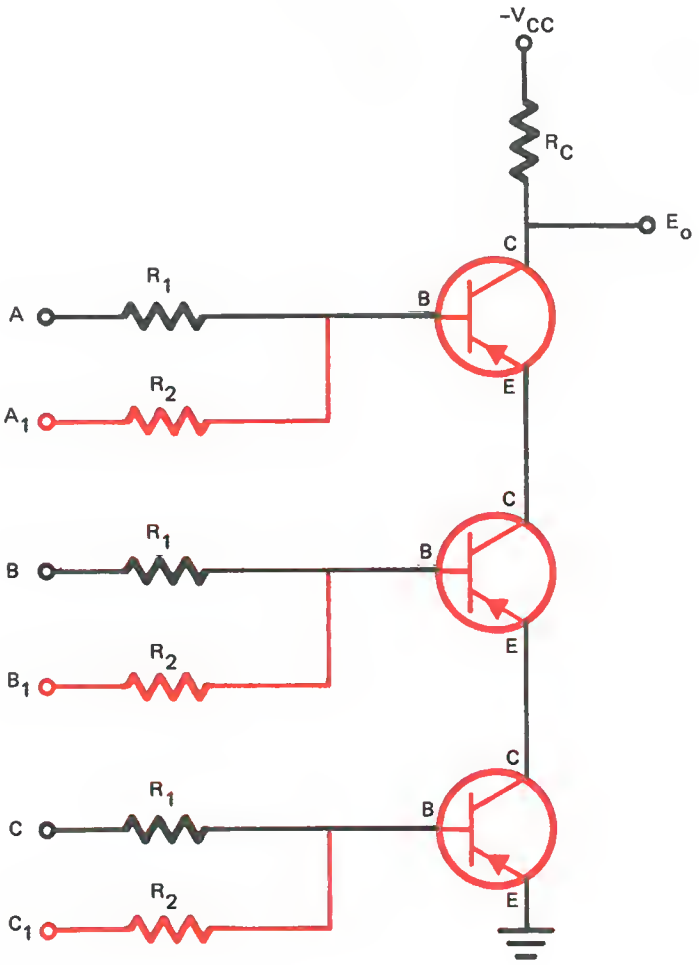


Fig. 12-2 Transistor Inhibitor Gate

As we have said, any time a positive going pulse of negative voltage arrives at the base of any of the transistors (Q_1, Q_2, or Q_3), that transistor will cut off and the output will drop to $-V_{CC}$. Suppose for some reason we wish to exclude certain pulses. For this we need to devise an inhibitor. Inhibitors are possible in both diode and transistor logic. The circuit in figure 12-2 is a transistor inhibitor gate.

Actually there are many ways for the gate action of the transistor to be inhibited. This circuit in figure 12-2 is only one of the ways. The transistors are normally on. They can be turned off by introducing a signal at A, B, or C which will change the bias and switch the transistor to cutoff. We can inhibit this action by applying signals at A_1, B_1 or C_1 to prevent the change in bias and thus keep the transistor on and prevent a shift in the output. These pulses can be chosen to prevent (or inhibit) at any given desired time. As with the other gates, changing the polarities of V_{CC} and inverting the signals will allow us to use NPN or PNP transistors and either positive or negative logic.

Many other types of inhibitor circuits can be constructed. The idea of inhibition can be

applied to OR, NOR, AND, and NAND circuits, and it simply means to block the gate, thereby preventing a change in output due to the incoming pulse. The inputs required usually have opposite levels, and the inhibitor signal causes the logic signal to have no effect (it is inhibited). The Boolean equation for the circuit will vary depending on which gate is inhibited. In the case of the series NOR gate shown in figure 12-1, the Boolean expression is equation 12.1.

$$A + B + C = -E_o$$

and would become

$$\bar{A} + B + C = -E_o \qquad (12.3)$$

With an inhibitor signal at A_1

$$\bar{A} + \bar{B} + \bar{C} = -E_o \qquad (12.4)$$

when the other gates are inhibited.

Another form of the inhibitor circuit can be seen in figure 12-3. The output is 0 or "false" unless the A is zero and the B is

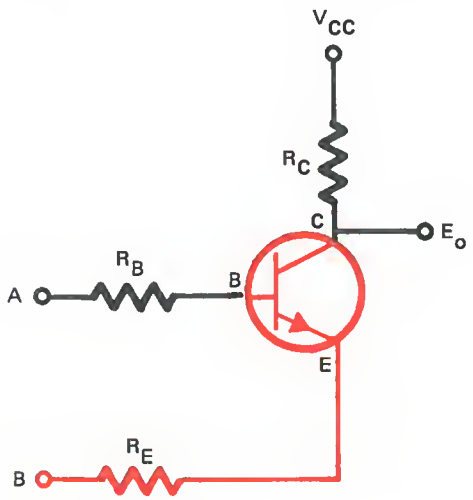


Fig. 12-3 Inhibited NAND Gate

one. Its Boolean expression is

$$AB = -E_o \qquad (12.5)$$

Its truth table is shown in figure 12-4.

A	B	$\bar{A}B = E_o$
0	0	10 = 0
1	0	00 = 0
1	1	01 = 0
0	1	11 = 1

Fig. 12-4 Truth Table for Inhibited NAND

The output of a NAND is inverted from that of an AND, so the Boolean expression for an inhibited AND is

$$\bar{A}B = E_o \qquad (12.6)$$

The logic symbol for an inhibited NAND gate is shown in figure 12-5.

The logic symbol for the series NOR gate in figure 12-1 is shown in figure 12-6. The alteration shown in figure 12-7 demonstrates the symbol for inhibiting one or more inputs. The symbol in figure 12-7 shows the A-gate inhibited.

Inhibitors are used with diode gates as well. Figure 12-8 shows a diode inhibitor gate. Its truth table, like the transistor inhibitor's, is the reverse of the normal gate. When A and B have no input and with a negative voltage at C (inhibitor signal), neither of the A or B diodes will conduct if the inhibitor signal is sufficient to hold the diode C at cutoff. That is to say,

$$V_{RL} - V_1 = 0 \qquad (12.7)$$

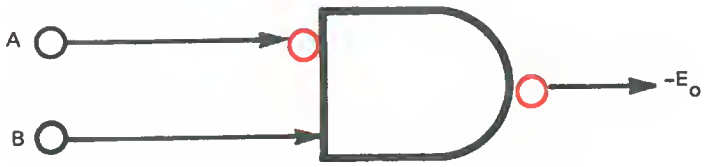


Fig. 12-5 Logic Symbol for Inhibited NAND Gate

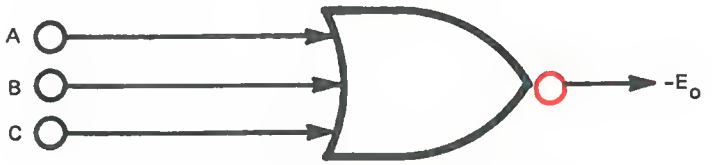


Fig. 12-6 Three Input NOR Gate

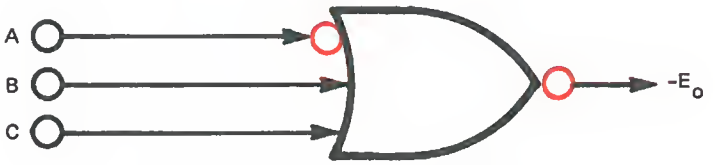


Fig. 12-7 Inhibited NOR Gate

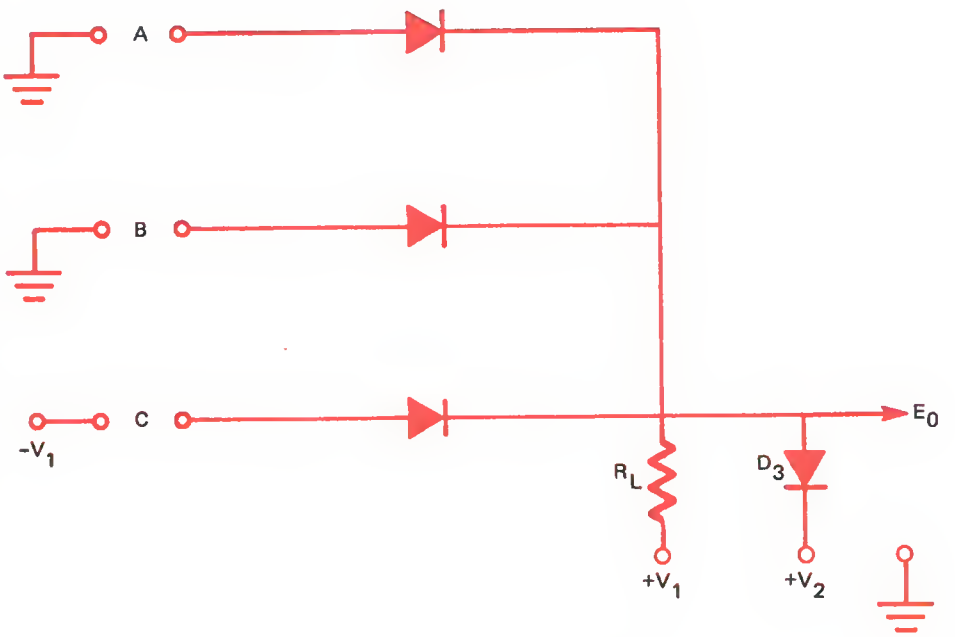


Fig. 12-8 Diode Inhibitor Gate

where V_{RL} is the drop across the load resistor R_L and V_1 is the bias voltage applied to R_L. The equation really says that the bias voltage (negative value) must be equal and opposite in order to cancel and hold diode C off.

With diodes A and B conducting, the clamp diode D_3 will conduct and clamp the output voltage to the V_2 value. When negative pulses are applied to A, the A-gate will cut off, but B will conduct and the output will remain clamped to V_2. The same thing happens when negative pulses appear at B with A conducting. If the pulses are applied to both A and B, both diodes will cut off, but the level can shift only to the value of $-V_1$ because there is no voltage from the diodes across R_L.

Inhibition occurs when a positive pulse is applied to C at the same time A and B receive negative pulses. In this case the diodes A and B will be cut off but C will conduct and nullify the A and B inputs. The diode C will cause a current to flow through the load and E_o cannot change.

MATERIALS

- 3 Transistors type 2N1304 or 2N1305 or equivalent
- 1 Set of output characteristics for the above transistors
- 3 Resistance substitution boxes (15Ω - 10 megΩ)
- 1 VOM or FEM
- 1 Oscilloscope
- 2 DC power supplies (0–40V)
- 8 Resistors, values to be determined by students
- 1 Breadboard
- 3 Transistor sockets
- 3 Semiconductor diodes, type 1N305 or equivalent
- 1 Function generator

PROCEDURE

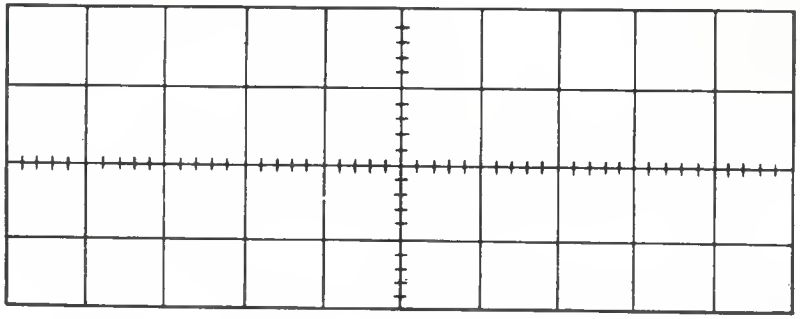
1. Choose a value of R_C which is appropriate for use with your transistor and a V_{CC} of 10 volts.
2. Compute a value of R_1 which is compatible with R_C and an E_S of 10 volts.
3. Construct a circuit similar to figure 12-1. Measure the output for no signal input with the VOM and oscilloscope.
4. Apply 1 kHz pulses of the correct polarity to A and record the results of the oscilloscope reading.
5. Repeat step 4 with pulses at B only and at C only.
6. Now try all the pulses at the same time. Record the results.
7. Construct a truth table for this circuit.
8. Select a value for R_2 and modify the circuit similar to that of figure 12-2.
9. Apply pulses to A, B, and C. At the same time, apply inhibitor pulses of the correct amplitude and polarity to A_1, B_1, and C_1. Record the results.

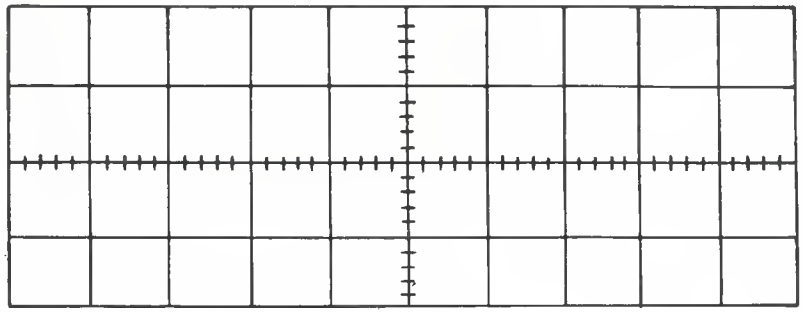
10. Remove the pulses from A_1. Record the results.
11. Remove the pulses from B_1. Record the results.
12. Remove the pulses from C_1. Record the results.
13. Construct a truth table for the fully inhibited circuit.
14. Disassemble the circuit and assemble a circuit similar to that shown in figure 12-8.
15. Calculate a value of R_L for $V_1 = 10$ volts.
16. Choose proper amplitude and polarity pulses to create a diode inhibitor gate. Record this circuit and then repeat steps 9 through 13.

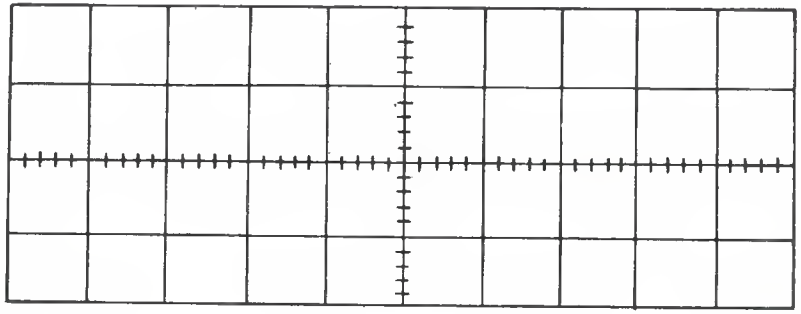
ANALYSIS GUIDE. In analyzing these data you should discuss the ways in which a gate can be inhibited. Some statement should be made as to the exact time the gate is inhibited and under what conditions. The results of the diode inhibitor should be compared with those of the transistor inhibitor. The uninhibited transistor gate should be compared with the inhibited gate.

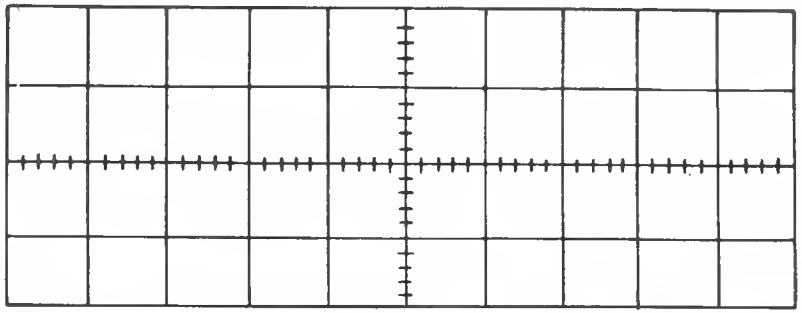
PROBLEMS

1. Draw a circuit for an inhibited series NAND gate. Show the truth table.
2. Show symbolically three, two-input NOR gates feeding a two-input NAND gate at the A input which is inhibited.
3. Write the Boolean expression for the network of problem two.





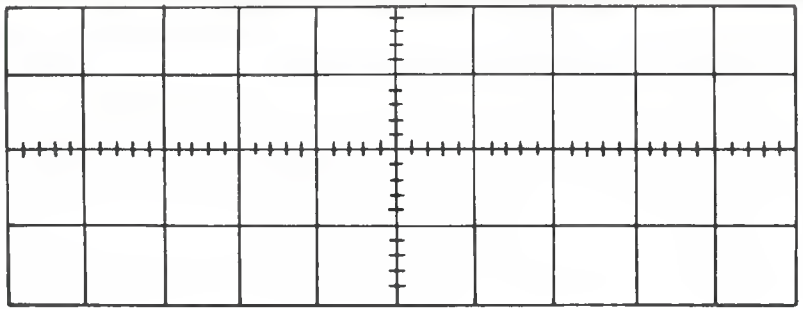


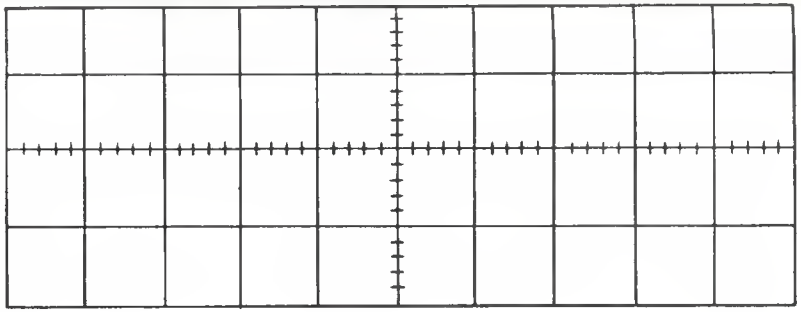


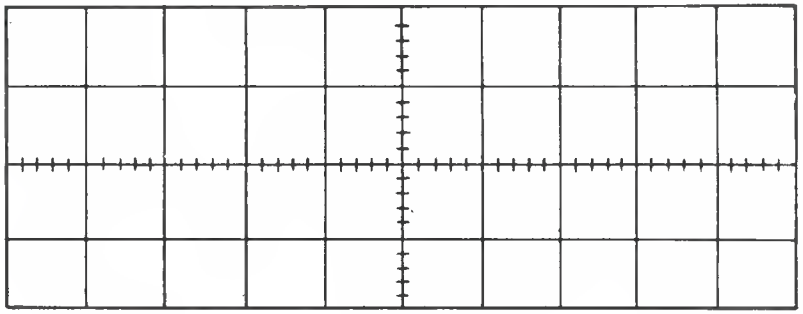
Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

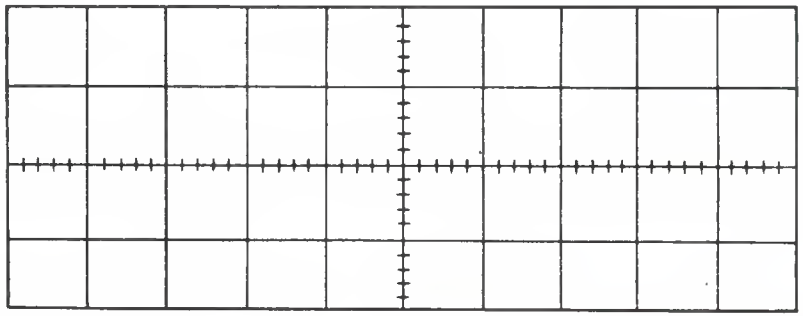
Show step numbers and output waveforms.
Give all relevant data such as amplitude,
period and reference level for each waveform.

Fig. 12-9 The Data Tables





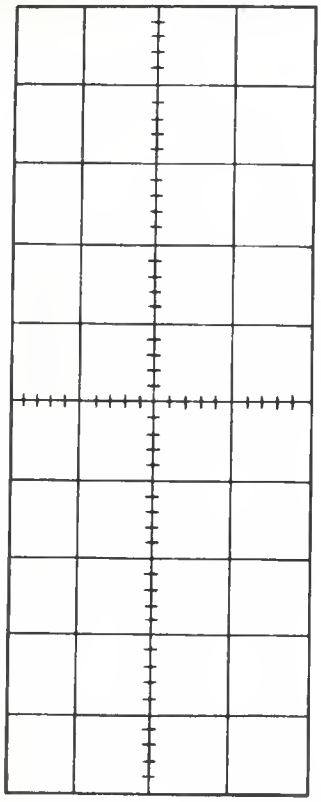




Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

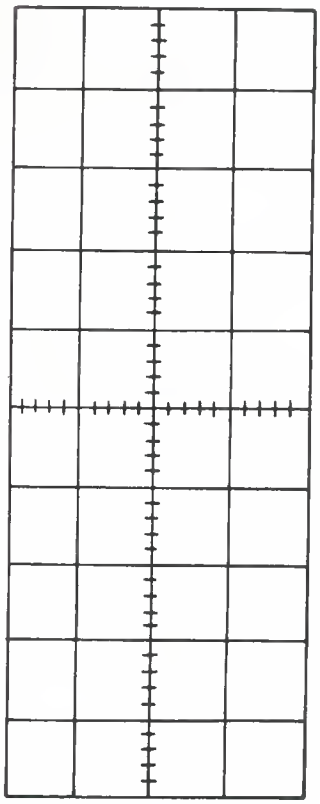
Show step numbers and output waveforms.
Give all relevant data such as amplitude,
period and reference level for each waveform.

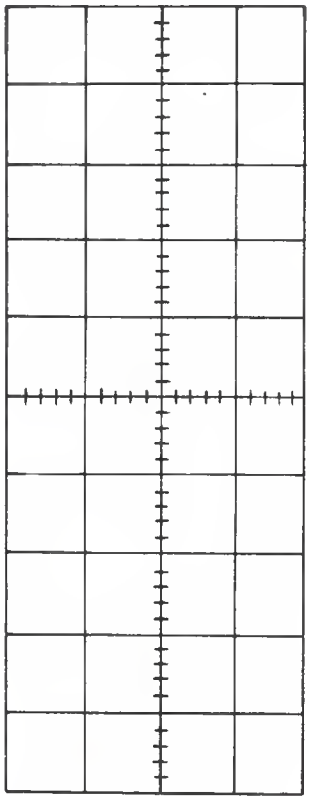
Fig. 12-9 The Data Tables (Cont'd)



Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Show step numbers and output waveforms.
Give all relevant data such as amplitude, period and reference level for each waveform.





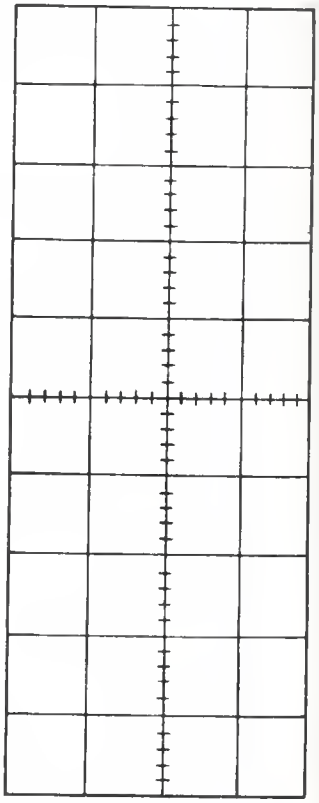


Fig. 12-9 The Data Tables (Cont'd)

INTRODUCTION. Multivibrator circuits consist of three basic types: astable, monostable, and bistable. The introduction to multivibrators will begin here with analysis of the astable and monostable multivibrator circuits.

DISCUSSION. The term multivibrator refers to a two-stage amplifier with positive *feedback*. As the names imply, an astable multivibrator, or free-running oscillator, has no stable condition, and the monostable, or one-shot, multivibrator has one stable condition.

Astable multivibrators, because of their output waveforms, are used as square wave generators, as frequency dividers, and for the timing of frequency. The design criteria for multivibrators is the same as for Class A amplifiers with the addition of a positive feedback loop. Figure 13-1 shows a basic astable multivibrator circuit. For symetrical operation, $R_{B2} = R_{B4}$ while $R_{B1} = R_{B3}$, and $R_{L1} = R_{L2}$. This allows each transistor to be ON for alternate half periods.

Selection of the component values for figure 13-1 will be made by a step-by-step procedure. Characteristic curves such as those shown in figure 13-2 (I_C vs V_{CE} and I_B vs V_{BE}) will be necessary.

Step 1. A current corresponding to point A can be chosen by the designer, and the load line (V_{CC} to I_{CMAX}) may intersect the maximum power dissipation curve. The resistance of this load line is V_{CC}/I_{CMAX}, where I_{CMAX} is the short circuit I_C. Since R_E is not bypassed, this resistance adds to the total collector circuit resistance. Thus

$$R_T = R_E + R_L \qquad (13.1)$$

Normally R_E is usually about 10 percent or less of R_T.

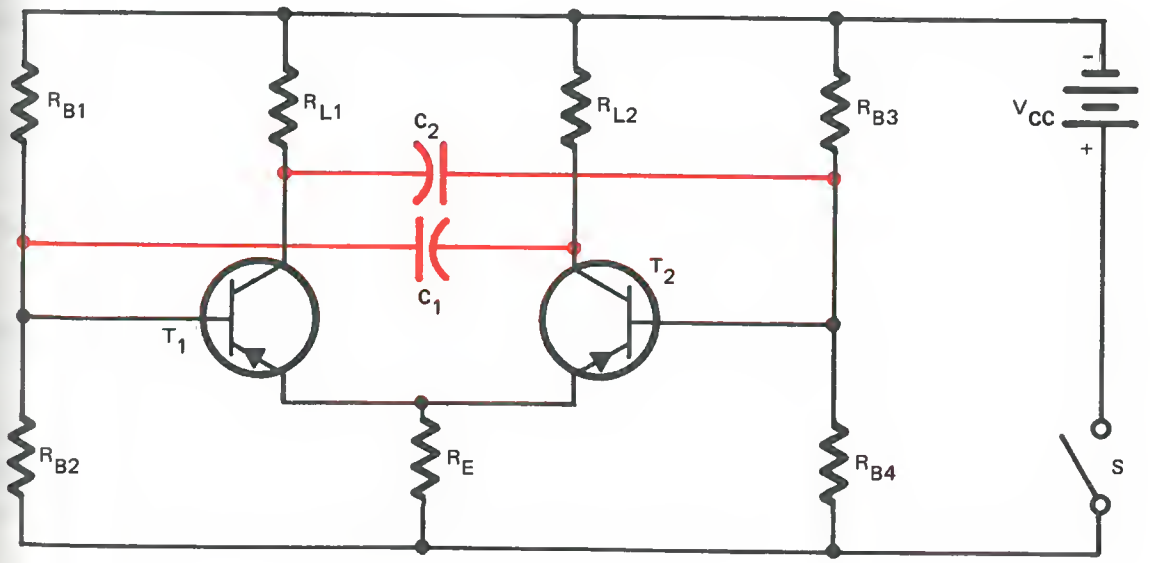


Fig. 13-1 Basic Astable Multivibrator

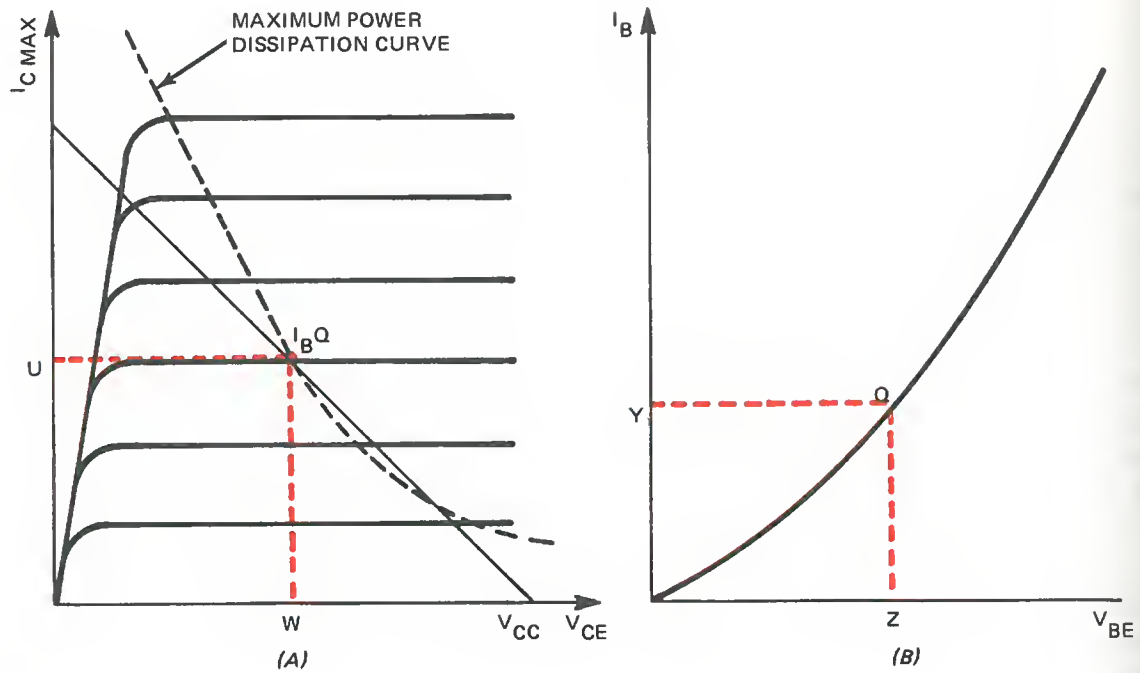


Fig. 13-2 Transistor Characteristics

Step 2. The Q point may normally be selected by the designer, but it should be kept in mind that we are designing with Class A criteria so the Q point should be selected near the center of the most linear portion of the load line.

Step 3. Read from the curves the values of I_{BQ}, I_{CQ}, and V_{CQ}. They are the values at Q in figure 13-2.

Step 4. By transferring the value of I_{CQ} to the I_B vs V_{BE} curve, the value of V_{BEQ} may be read directly (point Z on figure 13-2B).

Step 5. To determine R_{B2} the forward bias on the base of T_1 is provided by V_{RB2}. Also V_{BEQ} is required to forward bias the base of T_1 (V_{BEQ} was found in the above step). Since V_{BEQ} is a reverse bias, V_{RB2} must be large enough to offset V_{RB2Q} and still equal V_{BEQ}. The equation relating this requirement is

$$V_{RB2Q} = V_{REQ} + V_{BEQ} \qquad (13.2)$$

$$V_{REQ} = I_{EQ}\,(R_E) = (I_{CQ} + I_{BQ})\,R_E \qquad (13.4)$$

Note that the current through R_{B2} at rest will enhance thermal stability, but more bleeder current indicates a smaller R_{B2}, thus resulting in a reduction of input resistance. Therefore, the advantage is limited. As a rule of thumb, let

$$I_{RB2Q} = I_{BQ} \qquad (13.5)$$

Now calculation of R_{B2} may be found from

$$R_{B2} = \frac{V_{RB2Q}}{I_{RB2Q}} = \frac{V_{REQ} + V_{BEQ}}{I_{RB2Q}} \qquad (13.6)$$

Step 6. To determine R_{B1}, it is seen that R_{B1} and R_{B2} form a voltage divider across V_{CC}. Since V_{RB2Q} has been determined previously, then

$$V_{RB1Q} = V_{CC} - V_{RB2Q} \qquad (13.7)$$

Current passing through R_{B1} equals $I_{BQ} + I_{RB2Q}$. Therefore,

$$R_{B1} = \frac{V_{RB1Q}}{I_{RB1Q}} \qquad (13.8)$$

$$R_{B1} = \frac{V_{RB2Q}}{I_{RB2Q}} \qquad (13.9)$$

For symmetrical operation, recall $R_{B1} = R_{B3}$, $R_{B2} = R_{B4}$, and $R_{L1} = R_{L2}$, but due to variability of components, the value of R_{B2} and R_{B4} may be adjusted to bring V_C of both transistors to the value determined in step 3.

The determination of the value of the capacitors depends on the frequency of oscillations required. The cross-coupling capacitors affect the RC time constant, thus affecting the frequency of oscillations. An empirically derived formula may be used either to determine the frequency of oscillations, or to evaluate the capacitors if a definite frequency is desired.

$$f \cong \frac{1\,(10^6)}{0.025C + 2.5} \qquad (13.10)$$

where *C is the cross-coupling capacitor in pF.*

A *nonsymmetrical astable multivibrator* may be designed by causing one transistor to oscillate for a greater time than the other. This is accomplished by changing the values of the coupling capacitors, making C_1 and C_2 different values.

In the case of a monostable, one-shot, multivibrator there is only one stable state, one transistor ON while the other is OFF. For reliable timing, the ON transistor should be designed for saturation operation. When an externally applied pulse turns the ON transistor OFF, this forces the OFF transistor ON. Upon being driven into an unstable condition by the external pulse, the feedback network automatically begins to bring the circuit back to its stable state.

Referring to figure 13-3, let's again do a step-by-step procedure for the one-shot multi-

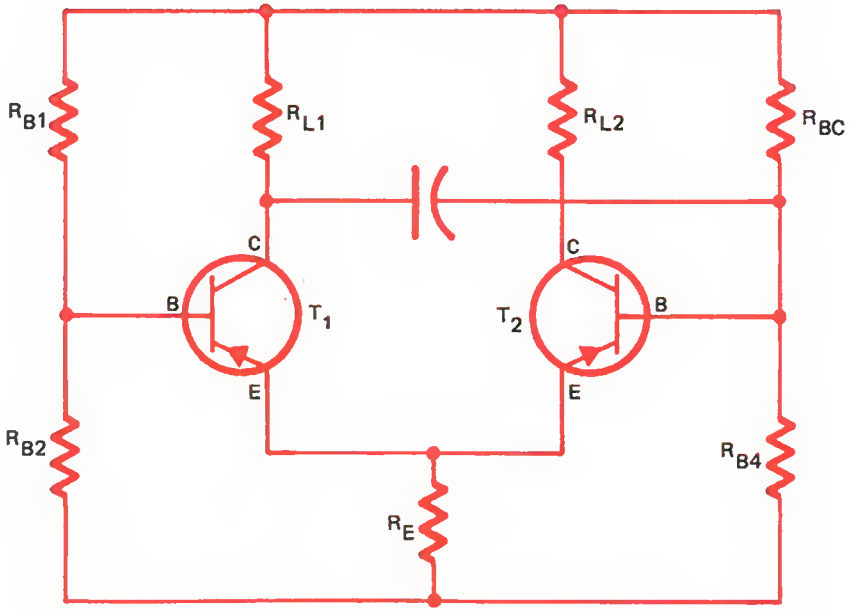


Fig. 13-3 A Basic Monostable Multivibrator

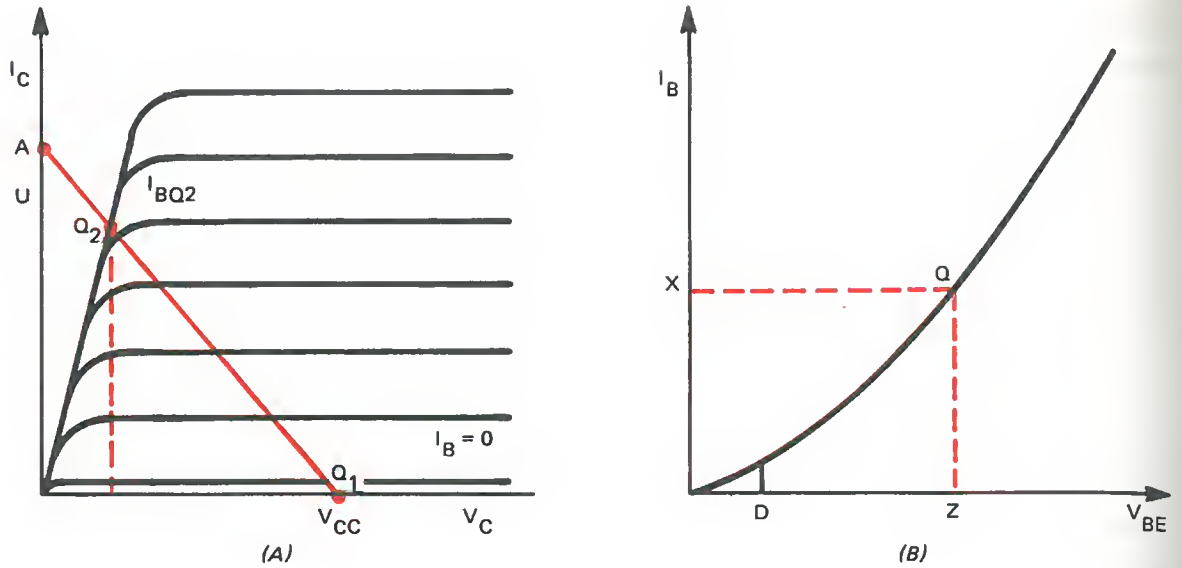


Fig. 13-4 Transistor Characteristics

vibrator, similar to the one for the astable multivibrator. The transistor characteristics will be helpful in this effort. Monostable characteristic design will correspond to the points given in figure 13-4 A and B.

Step 1. Here we chose $R_{L1} = R_{L2}$ (this is not necessary and for unequal R_{Ls}, separate load lines must be drawn). The same procedure can be used for determining the load line as was presented for the astable design:

$$R_T = V_{CC}/I_{CMAX} \qquad (13.11)$$

$$R_T = R_{L1} + R_E = R_{L2} + R_E \qquad (13.12)$$

$$R_{L1} = R_{L2} = R_T - R_E \text{ (Again } R_E \leqslant 10\% R_T) \qquad (13.13)$$

$$R_{B3} = \frac{V_{RB3Q}}{I_{RB3Q}} = \frac{V_{CC} - V_{RB4Q}}{I_{RB4Q} + I_{BQ}(T_2)} \qquad (13.27)$$

Again, R_{B2} and R_{B4} may be adjusted due to variability of parameters until the correct V_C is obtained on both transistors. The value of C_1 is chosen so as to get a desired amount of time in the unstable state. The larger the C_1 value, the longer the multivibrator remains in the unstable state. For this reason the circuit is used to standardize nonstandard random-timed pulses to be fed to computer circuits.

MATERIALS

- 1 Oscilloscope
- 1 Variable DC power supply (0-40V)
- 2 Transistors, type 2N1305 or equivalent
- 1 Set characteristic curves for the transistor used
- 2 Transistor sockets
- 1 Function generator
- 2 Capacitor substitution boxes
- 1 220Ω 1/2 watt resistor
- 2 Resistance substitution boxes (15Ω - 10 megΩ)
- 2 100 kΩ or 50 kΩ potentiometers (1W)
- 2 2.2 kΩ 1/2 watt resistors
- 1 0.01 μF capacitor
- 2 47 kΩ 1/2 watt resistors
- 1 Breadboard

PROCEDURE. $R_{L1} = R_{L2} = 2.5\ k\Omega$, $R_{B1} = R_{B3} = 100\ k\Omega$, $R_E = 200\Omega$

1. Construct the circuit shown in figure 13-1 using 100 kΩ potentiometers for R_{B2} and R_{B4}. **Do not connect C_1 and C_2 until Step 3.** T_1 and T_2 are 2N1305s and $V_{CC} = 12V$.
2. Start with $R_{B2} = R_{B4} = 30\ k\Omega$ and adjust resistance values until $V_{C1} = V_{C2}$.
3. Connect C_1 and C_2 and observe the output across T_2. Make a sketch of it.
4. Double C_1 and note what happens.
5. Slightly vary one of the potentiometers and observe any change in output.
6. Measure the frequency of the output and record it.
7. Disconnect the circuit and construct the circuit shown in figure 13-5.

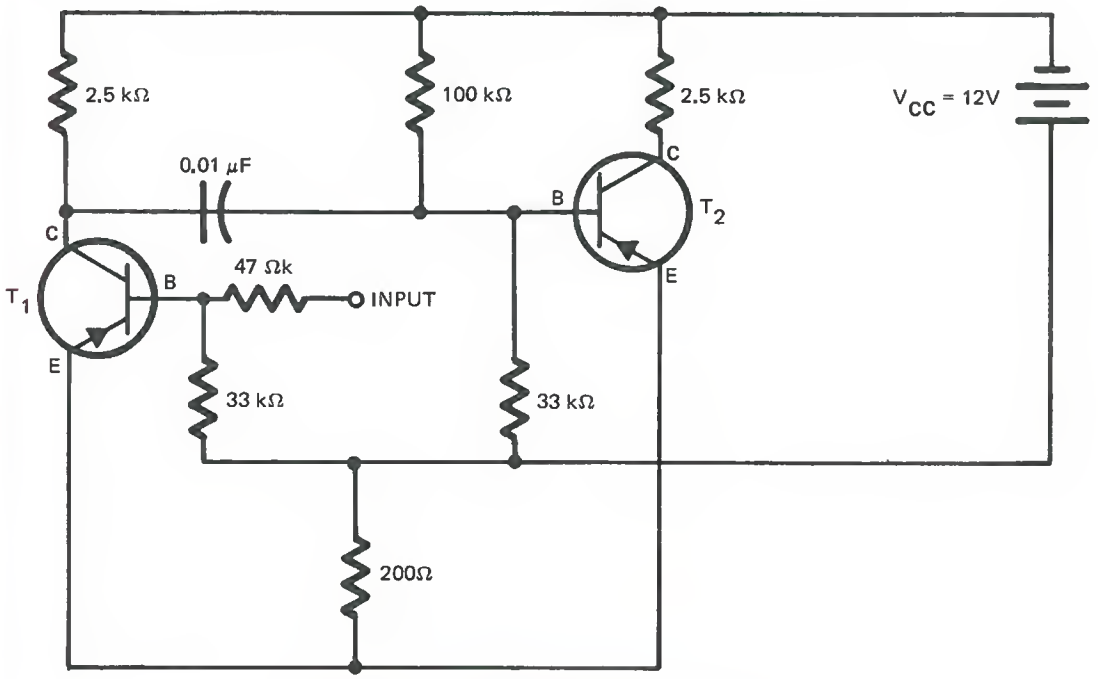


Fig. 13-5 The Experimental Circuit

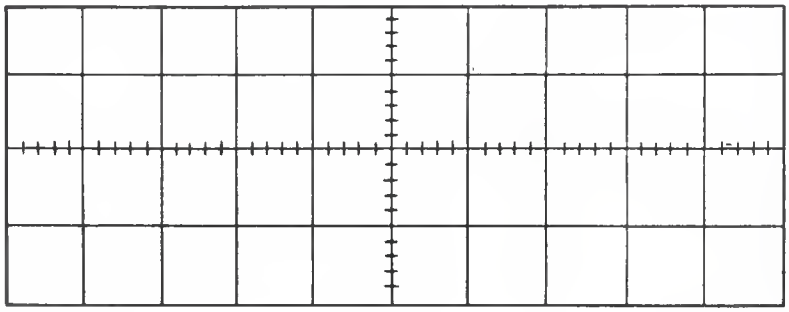
8. Connect a 5 $V_{p\text{-}p}$ 1000 Hz positive pulse signal to the input and observe the output.
9. Notice any effect a change in pulse duration has on the output. Also notice any effect the frequency of pulses has.
10. Vary the value of the capacitor and note any change in the output waveform.

ANALYSIS GUIDE. In analyzing this data you should discuss the operation of the astable and monostable multivibrator circuits. A comparison of input and output waveforms will be helpful in clarifying your discussion. Explain any changes in waveform that you observed in steps 4, 5, 9, and 10.

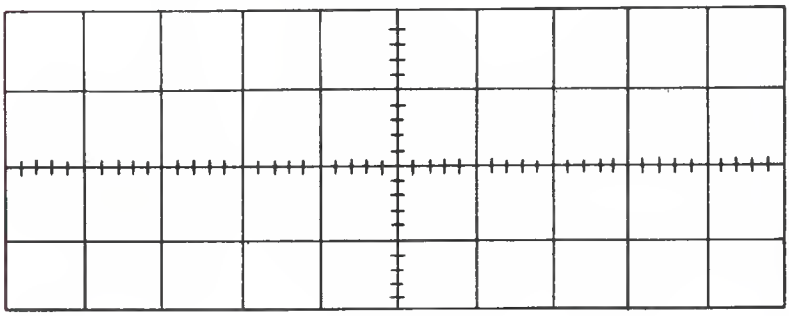
PROBLEMS

1. Calculate the frequency of oscillation of the circuit of the astable multivibrator and compare it with the observed result from step 6.
2. Explain how the output changed during step 4.
3. Did the base resistors change the output waveform in step 5? If so, how do you explain what occured?

f _____



Output Waveform of First Circuit



Output Waveform of Second Circuit

INTRODUCTION. In this experiment the bistable type of multivibrator circuit will be examined. Some basic design criteria for the bistable or "flip-flop" multivibrator will be presented.

DISCUSSION. In a bistable multivibrator, there are two stable conditions of operation: for example, T_1 saturated and T_2 cutoff, or T_1 cutoff and T_2 saturated. Either condition will last indefinitely unless an external signal is used to trigger the device into the opposite state. The bistable multivibrator is also known as the Eccles-Jordan trigger circuit, named after its inventors. The name "flip-flop" circuit is also commonly used. Bistable multivibrators are often used in a computer for electronic counting. Sometimes the bistable circuit is called a "trigger" because it starts other circuit actions, or a "binary" because it is used in binary counting systems.

Figure 14-1 shows a typical PNP bistable multivibrator circuit. Direct coupling and commutating capacitors are used between the two active devices. With the application of V_{CC} one transistor will normally draw more current than the other transistor. This forces the second transistor into the OFF state. For the purposes of this discussion, let's suppose that transistor T_1 is initially in conduction. The resistance of the ON transistor will be very small compared to R_3, and because of their voltage-divider action, the collector potential will be close to ground potential (zero). Referring to figure 14-1, notice that the base bias of T_2 depends on the collector potential of T_1 and on the relative values of R_6 and R_2.

With the lower end of R_3 very near to zero potential, T_2 will be cut off. With T_2 cut off, the voltage V_{C2} will approach $-V_{CC}$. R_4, R_5 and R_1 form a voltage-divider network

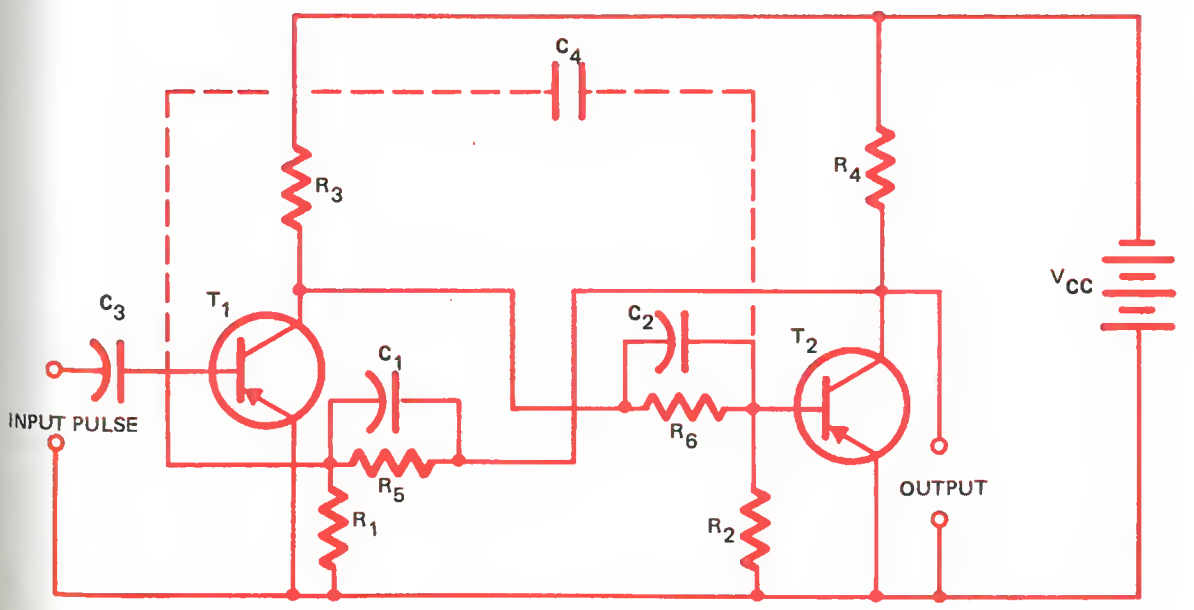


Fig. 14-1 Bistable Multivibrator

across V_{CC} and the values of these components are selected so as to maintain a negative potential at the base of T_1 which will keep it in the ON condition. When these conditions are satisfied, the circuit is in one of its stable states and will remain there so long as the conditions are not altered.

To change the stable state of the circuit a positive pulse can be applied to T_1 through the input capacitor C_3. This triggering pulse applied to the base of T_1 will cause conduction through T_1 to start decreasing, and this will cause the collector of T_1 to go from the zero potential value toward the $-V_{CC}$ value. This action will cause the base voltage of T_2 to change in the negative direction. If the application of the input pulse is long enough and of great enough amplitude, the base of T_2 will become sufficiently negative that T_2 will become forward biased. As T_2 begins to conduct, the collector voltage V_{C2} becomes less negative and tends to go toward ground (zero) potential. This is the potential being applied to the base of T_1. This reduction of negative base potential causes T_1 to conduct even less and this action of T_2 conducting more and T_1 conducting less is cumulative, with the final result being T_2 in saturation and T_1, cut off. The transistor circuit has then reached its other stable state, T_1 OFF, T_2 ON. If another positive pulse is applied to the base of T_1 through C_3, nothing will happen as a positive pulse only drives T_1 further into cut off.

For another positive pulse to cause the state to change, a capacitor C_3 (shown by dotted lines in figure 14-1) would be required. Then each positive pulse that is applied will cause one reversal of the multivibrator's state. Two negative pulses or a positive and a negative pulse could also cause a reversal of the stable state. This is sometimes not a desired reaction and additional circuitry can be used to insure that an unwanted signal does not trigger the multivibrator.

Now let's remove the commutating capacitors and relabel the resistors in order to consider some design criteria for the circuit. This has been done in figure 14-2.

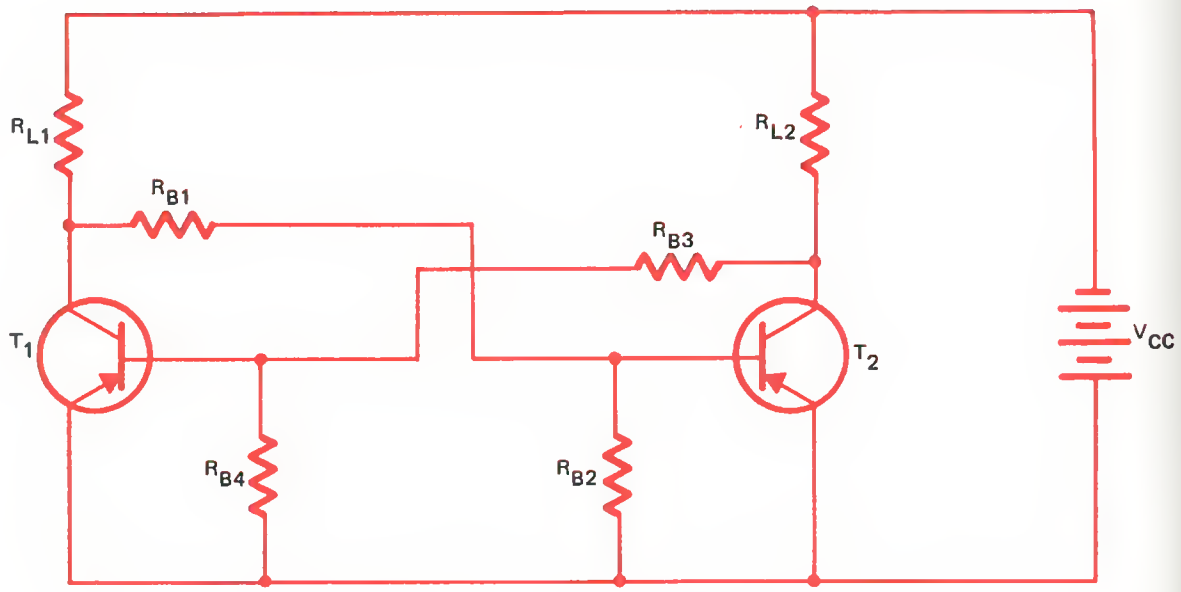


Fig. 14-2 Basic Bistable Multivibrator

After V_{CC} and R_L have been determined in the usual manner using collector curves and load line construction, let's assume that T_1 is ON and T_2 is OFF for the first stable state. In this condition

$$I_{C1} = \frac{V_{CC}}{R_{L1}} \qquad (14.1)$$

$$I_{B1} = \frac{I_{C1}}{\alpha_F} \qquad (14.2)$$

Substituting,

$$I_{B1} = (V_{CC}/R_L)\,\alpha_F = \frac{V_{CC}}{R_L\,\alpha_F} \qquad (14.3)$$

From the circuit of figure 14-2 we notice that

$$I_{RB3} = I_{B1} + I_{RB4} \qquad (14.4)$$

$I_{C2} = 0$ since T_2 is cut off. So

$$I_{RB3} = \frac{V_{CC} - V_{BE}\,(T_1\ ON)}{R_{B3} + R_{L2}} \qquad (14.5)$$

and

$$I_{RB4} = \frac{V_{BE}\,(T_1\ ON)}{R_{B4}} \qquad (14.6)$$

Substituting the equivalent values from the above equations,

$$\frac{V_{CC} - V_{BE}\,(T_1\ ON)}{R_{B3} + R_{L2}} = \frac{V_{CC}}{R_{L1}\alpha_F} = \frac{V_{BE}\,(T_1\ ON)}{R_{B4}} \qquad (14.7)$$

From this we get an expression for R_{B4}.

$$R_{B4} = \frac{R_{L1}V_{BE}(T_1\ ON)\alpha_F(R_{L2} + R_{B3})}{V_{CC}R_{L1}\alpha_F V_{BE}(T_1\ ON) - V_{CC}R_{L2} - V_{CC}R_{B3}} \qquad (14.8)$$

If we were dealing with a symmetrical multivibrator, $R_{B2} = R_{B4}$, and $R_{B3} = R_{B1}$. If not, the same procedure would be used to compute the unknown resistances. Since R_L, V_{BE}, (T_1 ON) α_F and V_{CC} were treated as constants, the variation of R_{B3} and R_{B4} may be plotted by use of the equation for R_{B4}.

For T_2 being OFF, the I_{CO} of this transistor often may not be neglected.

$$V_{BE}\,(T_2\ OFF) = (I_{bleeder} - I_{CO})\,R_{B2} \qquad (14.9)$$

The current through R_{B1} is

$$I_{RB1} = \frac{V_{CE}\,(T_1\ ON) - V_{BE}\,(T_2\ OFF)}{R_{B1}} - I_{CO} \qquad (14.10)$$

So

$$\frac{V_{BE}\,(T_2\ OFF)}{R_{B2}} = \frac{V_{CE}\,(T_1\ ON) - V_{BE}\,(T_2\ OFF)}{R_{B1}} - I_{CO} \qquad (14.11)$$

or

$$R_{B2} = \frac{V_{BE}\,(T_2\ OFF)\,R_{B1}}{V_{CE}\,(T_1\ ON) - V_{BE}\,(T_2\ OFF) - I_{CO}R_{B1}} \qquad (14.12)$$

and, as before, R_{B2} vs. R_{B1} can be plotted.

Remember the capacitors C_1 and C_2 in figure 14-1? The main purposes of the capacitors were to;

1. Reduce the recovery time.
2. Reduce the transition time (which, in turn, reduces the minimum pulse width).

That is, capacitors C_1 and C_2 provide base overdrive for pulse shaping and faster switching time.

MATERIALS

1 Oscilloscope
2 Resistance substitution boxes (15Ω - 10 megΩ)
2 Transistors type 2N1305 or equivalent
2 Capacitor substitution boxes
2 2.5 kΩ 1/2 watt resistors
2 33 kΩ 1/2 watt resistors
1 200Ω 1/2 watt resistor
2 Variable DC power supplies (0-40V)
1 Multimeter
2 0.01 μF capacitors
1 Breadboard
2 Transistor sockets
1 Function generator
1 SPDT switch

PROCEDURE

1. Construct the circuit in figure 14-3. Have your lab partner check the circuit before you apply the V_{CC}. Use the resistance substitution boxes for the base coupling resistors (47 kΩ).

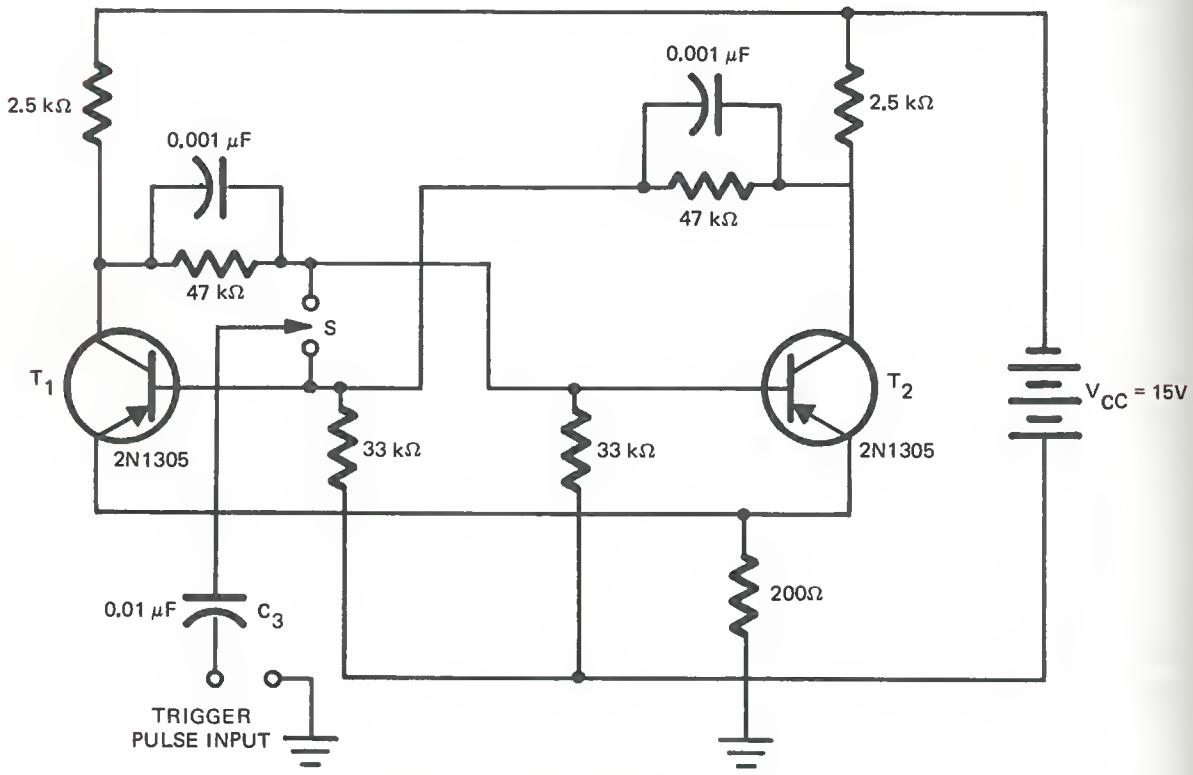
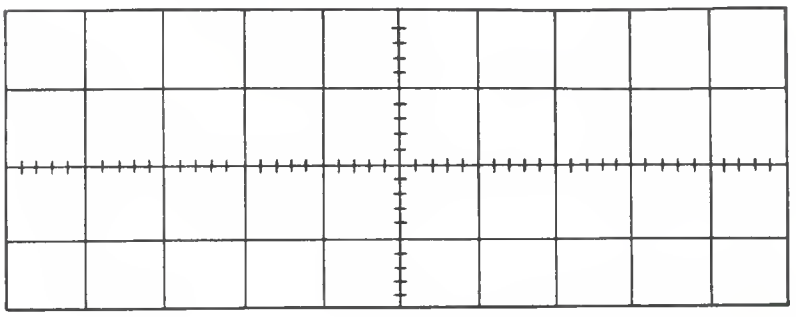


Fig. 14-3 The Experimental Circuit

2. Measure and record the voltages, V_{C1} and V_{C2}.
3. Determine from the above measurements which transistor is conducting and which one is OFF.
4. Apply a positive 3 volts to the base of the ON transistor through the switch and C_3. Momentarily close the switch to do this.

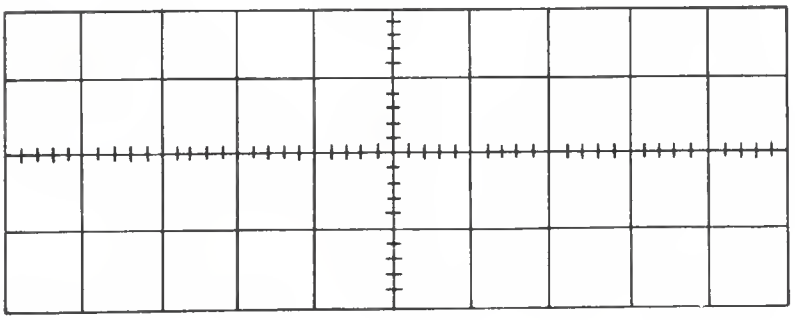
V_{C1} = _____

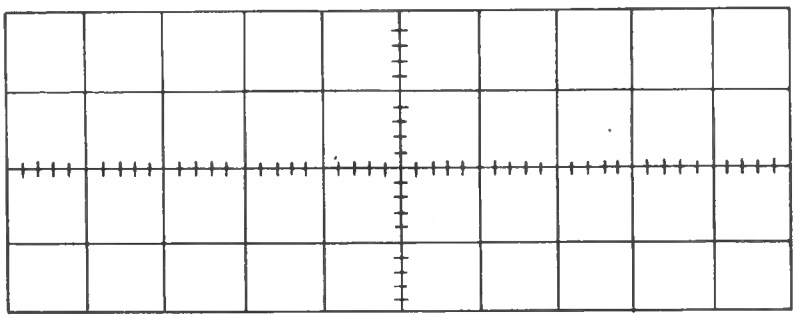
V_{C2} = _____



V_{C1}' = _____

V_{C2}' = _____





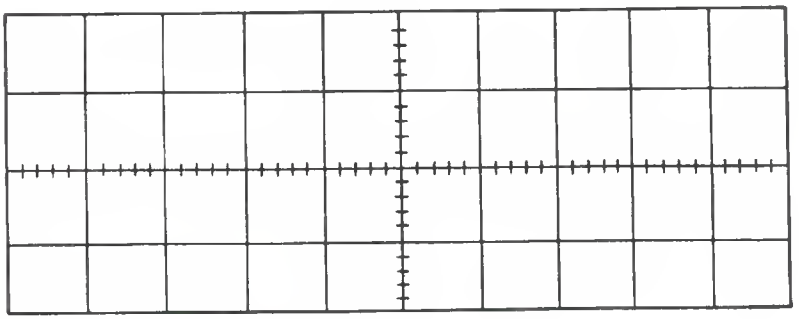


Fig. 14-4 The Data Table

5. Measure and record V_{C1}' and V_{C2}' again and determine whether the circuit switched stable states. If the answer is no, then repeat steps 2, 3, and 4 using a five-volt positive signal.

6. Connect the oscilloscope to view V_{C2} and put a pulse signal of about 1000 Hz through C_3 to the base of T_1. Also connect a 0.01 μF capacitor (as C_4 shown in figure 14-1) to drive the base of T_2.

7. Record the output waveform at V_{C2} and compute the frequency. Compare this with the input triggering frequency.

8. Vary the coupling resistances several steps up and down (the 47 kΩ on the resistance boxes). Then reset them to 47 kΩ and similarly vary the value of C_4. Be able to satisfy yourself that you know what is causing any change that you observe.

ANALYSIS GUIDE. In analyzing these results you should discuss the application of the basic circuit investigated to the basic design criteria presented. Operation of the circuit should be covered with regard to the design criteria, and with special attention given to the effect of varying the coupling.

PROBLEMS

1. How many stable states were there in the experimental circuit?

2. How did the output waveforms change when the value of the base coupling resistance was varied?

3. Explain how the experimental circuit could be used as a counter.

experiment 01111 MULTIVIBRATOR TRIGGER CIRCUITS

INTRODUCTION. General triggering power requirements and frequency limitations are very important to practical digital applications. In this experiment we will examine some of these factors. We will also look at a basic design criteria for a Schmitt trigger circuit.

DISCUSSION. To cause a multivibrator to change states we must apply a trigger signal to correct polarity and magnitude. Under normal operation the ON transistor is triggered OFF, because the time required to turn a transistor OFF is normally less than that required to turn an OFF transistor ON.

The trigger circuit must furnish a sufficient amount of power to dependably turn off the transistor. If the transistor is not saturated, then the trigger charge that must be supplied can be approximated by

$$Q_B \cong \frac{0.194\, I_C}{f_\alpha} \qquad (15.1)$$

where f_α is the alpha cutoff frequency. Any charge lower than Q_B will not dependably turn the transistor off. The time required to turn the transistor off may also be approximated.

$$t_{\text{turn OFF}} \cong \frac{(0.159)\, h_{FE}}{f_\alpha} \qquad (15.2)$$

If a quick turnoff time is required, then a glance at this equation indicates the use of a transistor with a high alpha cutoff frequency, or a low current gain can be used to reduce the turnoff time.

If the transistor to be switched is in saturation, then additional charge equal to the stored base charge of the transistor must be supplied by the trigger circuit.

$$Q_{trig} \cong Q_B + Q_{BS} \qquad (15.3)$$

where Q_{BS} = *stored base charge of the saturated transistor.*

In a practical multivibrator the coupling circuit capacitors also affect the time required for switching. If the trigger input is capacitively coupled, then reducing the capacitor size reduces the differentiated trigger pulse duration, allowing higher triggering rates to be used. This reduction in capacitor value is limited since the capacitor must handle the Q that is required at the base. Since

$$Q = V_{trig}\, C \qquad (15.4)$$

then

$$C_{min} = \frac{Q_B}{V_{trig}} \text{ (Nonsaturated Case)} \qquad (15.5)$$

or

$$C_{min} = \frac{Q_B + Q_{BS}}{V_{trig}} \text{ (Saturated Case)} \qquad (15.6)$$

Emitter triggering is the name applied to the technique of connecting the input trigger to the emitter of the transistor and is used most effectively at lower triggering frequencies. Figure 15-1 shows a typical emitter triggering circuit.

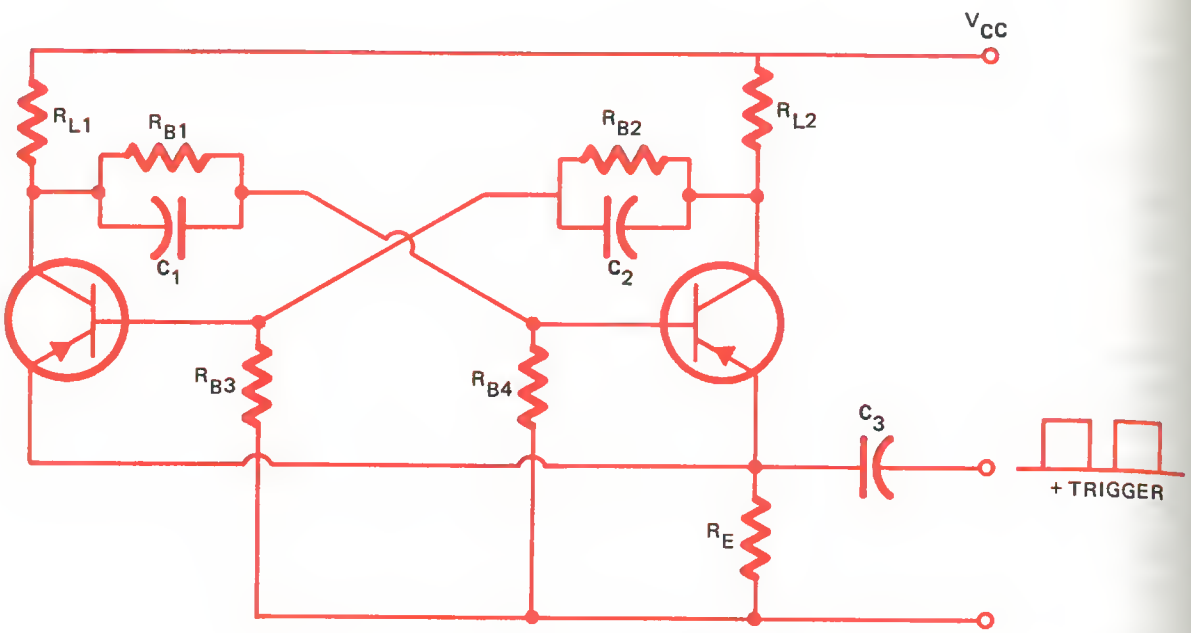


Fig. 15-1 Emitter Triggering

The frequency of the trigger is very important since all the capacitors should be at their normal state before the next trigger pulse is applied. For that reason, the pulse should be ON for at least 5 starting time-constants and OFF for at least 5 recovery-constants in order to insure proper triggering.

For base and collector triggering, the same basic requirements are necessary as for emitter triggering. A point to note about base triggering is that the signal frequency at the collector will be one-half the triggering frequency. Consequently, multivibrators are sometimes used to divide pulse rates by two. Rather large pulses are required to trigger a multivibrator at the collector. However, the output waveform with collector triggering is usually the most square of the three types.

$$R_{L1} = R_{L2};\ R_{B1} = R_{B2};\ R_{B3} = R_{B4};$$

$$C_1 = C_2 \qquad (15.7)$$

In figure 15-1 the circuit is constructed using PNP transistors and positive trigger pulses are used.

Let us turn our attention now to a special application of a bistable multivibrator which is common in computer circuitry, the Schmitt trigger. The chief uses of a Schmitt trigger are:

(1) To convert or reshape sinusoidal or rectangular waveforms
(2) To detect the presence of a signal.

Figure 15-2 is a basic Schmitt trigger and figure 15-3 is its associated waveforms.

The circuit in figure 15-2 is designed so that the stable state of T_2 ON and T_1 OFF will remain until an input signal of predetermined magnitude and polarity is applied to the base of T_1. When this signal is applied to the base, the circuit flips, and the other

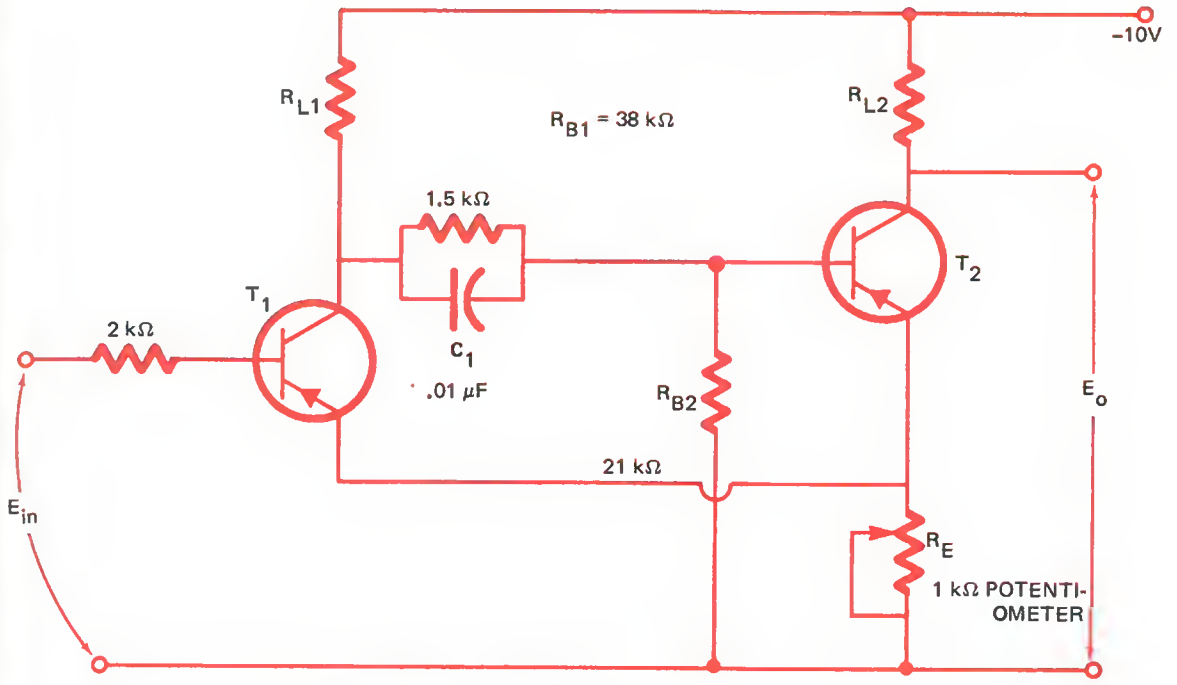


Fig. 15-2 A Schmitt Trigger Circuit

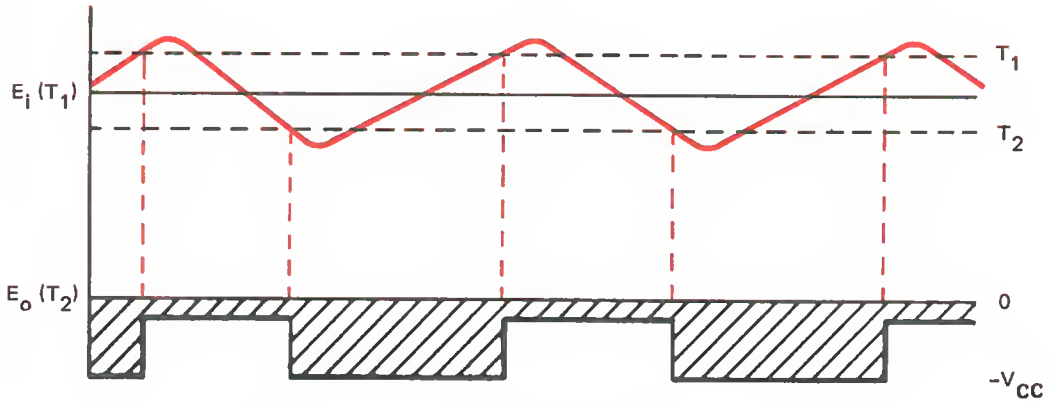


Fig. 15-3 Waveforms For a Schmitt Trigger

stable state will hold until a signal of the opposite polarity and sufficiently large is applied to the base of T_1 to shut it off again. By varying the potentiometer R_E, the trigger level at which the transistors change state may be changed.

We can determine circuit component values for the Schmitt trigger using the following process. The stable state of T_2 ON, T_1 OFF will be assumed, and the value of V_{BE}, (T_2 ON) must be known, as well as the value E_i, at which the circuit must flip.

$$V_{RE,\,Q} \cong V_{RB2,\,Q} - V_{BE,\,(T_2\ ON)} \qquad (15.8)$$

and

$$E_{i,\,min} = V_{BE,\,min\,(T_1)} + V_{RE,Q} \qquad (15.9)$$

For our circuit $E_{i,\ min} = -2V$ and $V_{BE,\ Q} = -0.2V$

This implies that $V_{RE,\ Q} = -1.8V$

We can solve for $V_{RB2,\ Q}$ if we know $V_{BE,\ (T_2\ ON)} = -0.3V$

Therefore,

$$V_{RB2,\ Q} = -2.1V \qquad (15.10)$$

If we select a bleeder current of say 10^{-4} amps, then

$$R_{B2} = \frac{V_{RB2,\ Q}}{I_{bleeder}} = 21\ k\Omega \qquad (15.11)$$

and

$$R_{B1} + R_{L1} = \frac{V_{CC} - V_{RB2,\ Q}}{I_{bleeder} + I_{B2,\ ON}} \qquad (15.12)$$

By choosing a value of R_{L1}, we may compute R_{B1}.

R_E may be computed if the h_{FE} of the transistor is known.

$$I_{C2,\ ON} = h_{FE}\, I_{B2,\ ON} \qquad (15.13)$$

and

$$I_{RE,\ Q} = I_{C2,\ ON} + I_{B2,\ ON} \qquad (15.14)$$

Therefore,

$$R_E = \frac{V_{RE,\ Q}}{I_{RE,\ Q}} \qquad (15.15)$$

R_{L2} may be determined by

$$V_{RL2} = V_{CC} - \left[V_{CE,\ (T_2\ ON)} + V_{RE,\ Q}\right]$$

$$R_{L2} = \frac{V_{RL2}}{I_{C2,\ ON}}$$

$$= \frac{V_{CC} - \left[V_{CE,\ (T_2\ ON)} + V_{RE,\ Q}\right]}{I_{C2,\ ON}}$$

With this in mind, using the obtained values, the circuit in figure 15-2 is ready for operation.

MATERIALS

- 1 Oscilloscope
- 2 Transistors type 2N1305 or equivalent
- 2 Transistor sockets
- 1 Function generator
- 1 2.2 kΩ, 1/2 watt resistor
- 1 Breadboard
- 3 Resistance substitution box (15Ω to 10 megΩ)
- 1 Capacitance substitution box
- 1 DC transistor power supply (0–40V)
- 1 2 kΩ potentiometer

PROCEDURE

1. Construct the circuit shown in figure 15-4 using your computed values of R_{L2} and R_E. Use a collector voltage of $V_{CC} = 10V$. Record your values on the diagram.
2. Apply a sinusoidal input of 1000 Hz and observe the amplitude necessary to trigger the circuit.

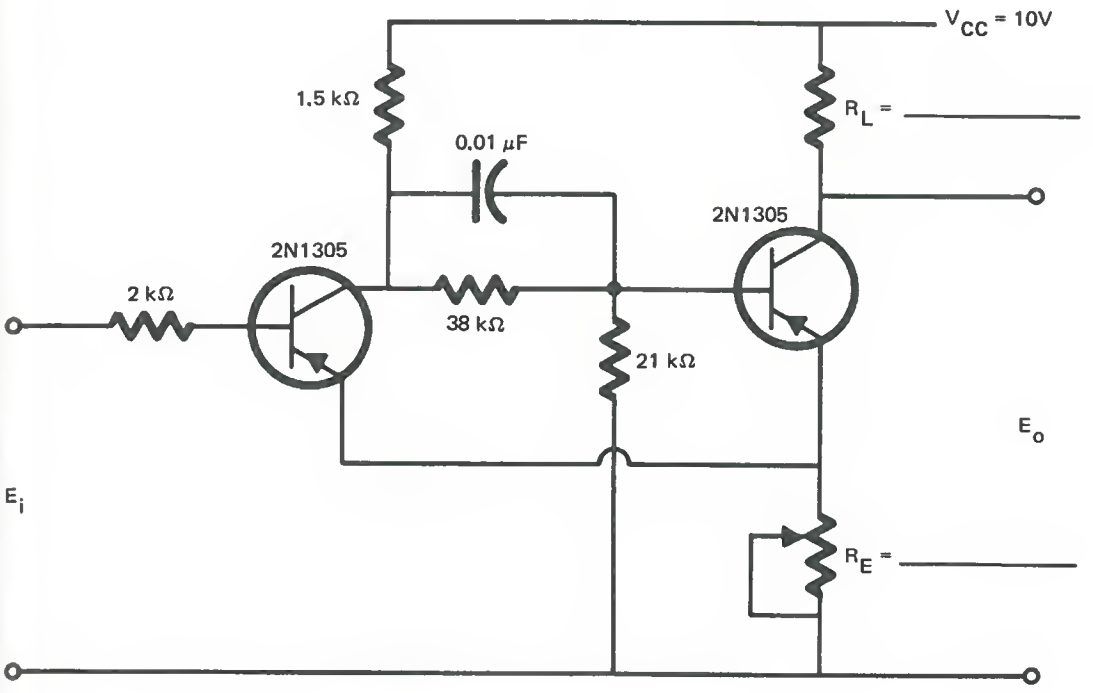
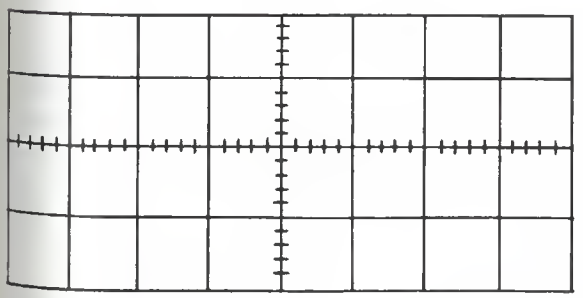


Fig. 15-4 The Experimental Circuit

3. When the input is triggering, determine the frequency of the input and output waveforms and record them.
4. Slowly increase the input frequency to 10,000 Hz and observe the output waveform.
5. Reset the input frequency to 1,000 Hz and vary the emitter resistor. Note any effect it has on the output.

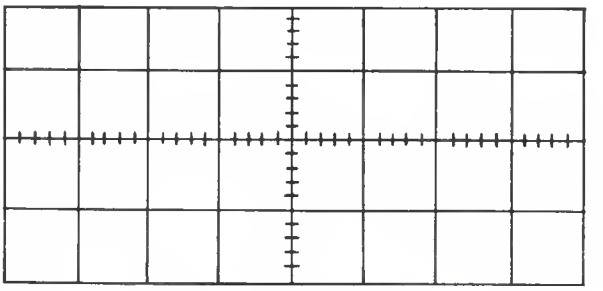
ANALYSIS GUIDE. In analyzing these results the general triggering considerations of the multivibrator should be discussed, including the power requirements and frequency limitations. Also discuss several practical applications for a Schmitt trigger circuit.

Input



f = _____

Output



f = _____

Fig. 15-5 The Data Tables

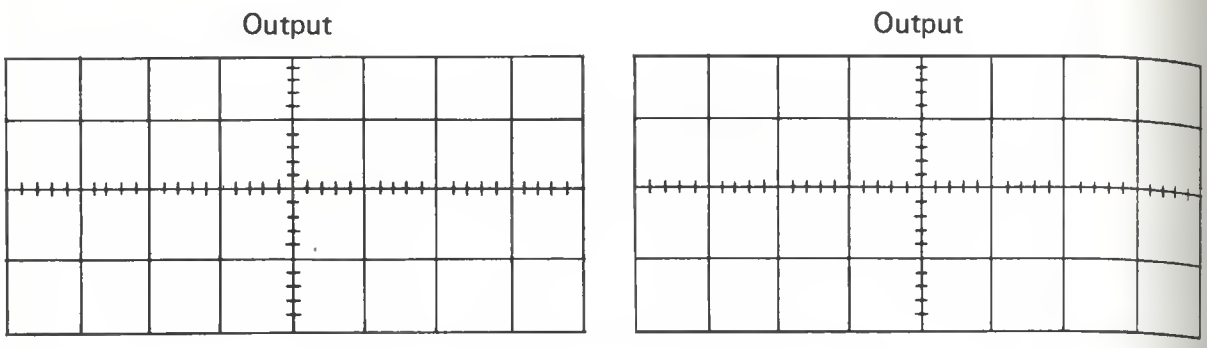


Fig. 15-5 The Data Tables (Cont'd)

PROBLEMS

1. In step 3 of the procedure, was the frequency out one-half the input frequency? Explain.
2. What effect did varying the emitter resistor value have?
3. Explain what happened as the input frequency was increased.

experiment 10000 INTEGRATED CIRCUIT LOGICAL FLIP-FLOPS

INTRODUCTION. Computers use literally thousands of multivibrators to perform their computations. In this experiment we are going to examine an integrated circuit flip-flop. We will consider how the operation of the IC is similar to that of a discrete component flip-flop circuit.

DISCUSSION. A modern computer makes its calculations by turning transistors ON and OFF. These transistors are arranged in many types of circuits, including shift registers, counters, ring counters, etc. These circuits can be considered building blocks for logical design. Counting circuits are made up of strings of multivibrators fed by gates, inverters, and triggers. The electronic signals are routed through the computer to the output devices (card punches, printers, tape, and disk storage) by these building-block circuits.

Back at the beginning of the electronic computer development, the most common devices available for constructing these building blocks were vacuum tubes. The idea was the same as for transistors but the size and requirements for vacuum tubes required much effort to be directed toward cooling the machine. All of these problems created a limitation in the practical handling capabilities of vacuum tube computers.

With the advent of the transistor, designers were able to greatly decrease the size, weight, and operating temperature of any given computer by simply using transistor multivibrators, diode gates, transistor gates, etc. The size reduction allowed more circuits in a given area and the capacity of the machine could be increased. The fast switching times of present transistors allow more computation per unit of time.

The integrated circuit carries some of these refinements to an even higher degree. Each integrated circuit module contains many of the components (or the equivalent) for a number of the discrete circuit building blocks.

For instance, a typical IC may contain several AND gates and some flip-flop (bistable multivibrators). A typical schematic representation appears in figure 16-1. This is a highly versatile building block that can be used in many applications. We can recognize the representation as being DTL logic. Figure 16-2 shows a logic symbol representation of this same circuit. Actually, the logic symbol representation is usually the most useful. Although the schematic is drawn using conventional symbols, the actual operation only approximates this circuit. It is enough to know that the circuit operates as the logic symbols indicate.

The bistable multivibrator is commonly called a flip-flop. The stable state of the circuit is not discernible from the diagram. Since both states (condition ON or OFF) are stable, the particular state is dependent on the application of a trigger pulse and the immediate past history of the circuit. We do know that in each state one of the transistors is in cutoff while the other is in saturation. Figure 16-3 shows a general circuit for a bistable multivibrator.

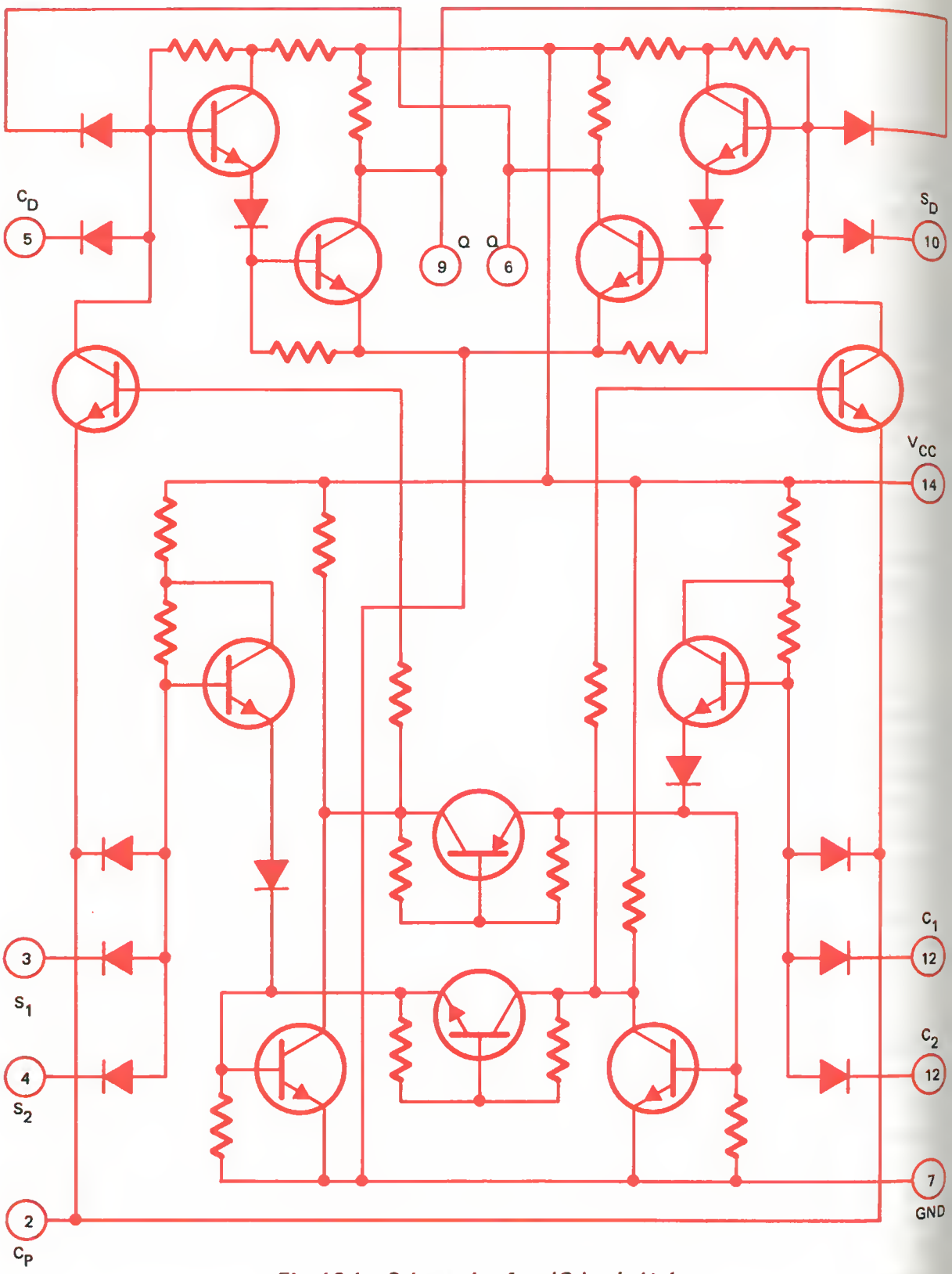


Fig. 16-1 Schematic of an IC Logic Unit

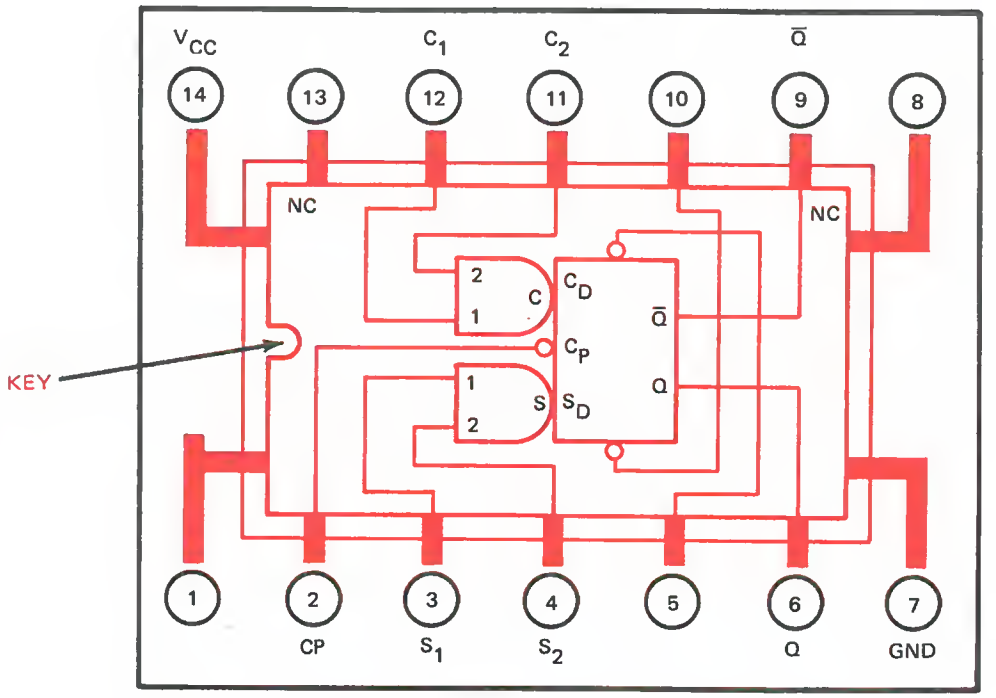


Fig. 16-2 Logic Symbol Representation of an IC Unit

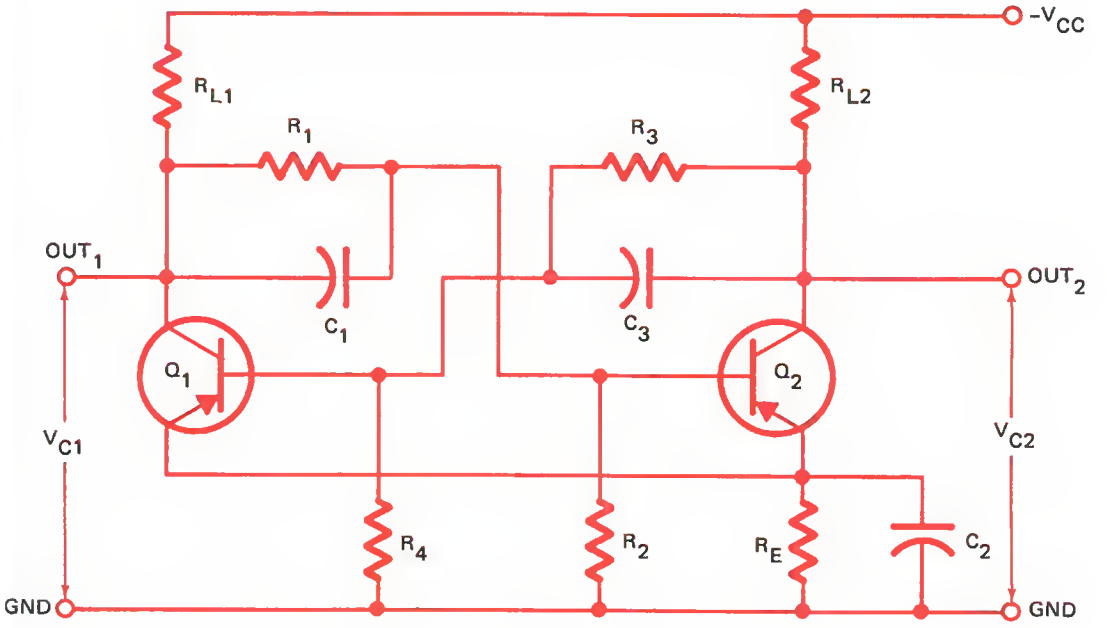


Fig. 16-3 A Bistable Multivibrator

If Q_1 is in saturation and Q_2 is at cutoff, then $V_{C2} = V_{CC}$ and $V_{C1} = V_E$. The voltage V_{B2} will be less than V_E. Capacitors C_1 and C_3 are speed-up capacitors. Capacitor C_2 serves to keep V_E constant during the transition from one state to the other.

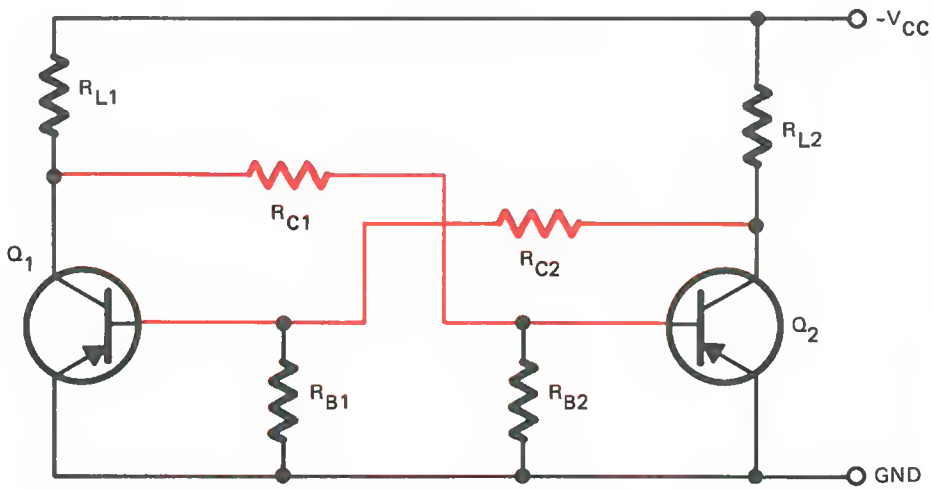


Fig. 16-4 Direct Coupled Flip-Flop

When a trigger pulse is applied so that Q_1 is driven to cutoff, the circuit changes to the other stable state where Q_1 remains in cutoff and Q_2 remains in saturation. Under these conditions, V_E remains unchanged, $V_{C1} = V_{CC}$, $V_{C2} = V_E$, and V_{B1} is less than V_E. Another trigger pulse would cause the circuit to revert to the first condition.

So we see that the flip-flop consists of two common emitter switches. The two are connected so that the output of the first is the input to the second, and the output of the second is the input of the first. Another general circuit is the direct-coupled bistable multivibrator of figure 16-4. The operation of this circuit is essentially the same as that described before. The circuit can be triggered by application of pulses of the proper magnitude and polarity to any one of the transistor terminals. An astable flip-flop may be symmetrical or nonsymmetrical in its output. That is, the ON and OFF times may or may not be equal. We may further classify flip-flops as to whether or not the transistor is allowed to go into saturation. The saturating type is the easiest to build, but its slow operation makes it less desirable in many practical applications.

Any basic flip-flop becomes a logic flip-flop when input and output circuits are added. Usually each side of the flip-flop will have two inputs. The first is a logic circuit input through multiple input gates. The other is a set or reset input which goes more or less directly into the switching device. There are usually two outputs, one labeled Q and the other not Q or $\overline{Q}$. The logic symbol for a NPN reset-set flip-flop is illustrated in figure 16-5. A clock input is usually present to provide automatic reset at a given clock frequency. This can be seen in figure 16-1 labeled C_P.

In the case of the NPN flip-flop, negative trigger pulses are applied to the *set* input when the flip-flop is in the opposite state and is to be brought back to the initial condition. When the reverse condition is desired, the negative pulses can be applied to the *reset* input and the bistable will switch states. The application of the negative signal pulses to the logic input or reset of Q_1 will flip it from 1 to 0. Negative pulses to logic input or set of T_2 will flip it from normal 0 state to 1. (These are labeled Set and Clear or S_D and C_D on many ICs).

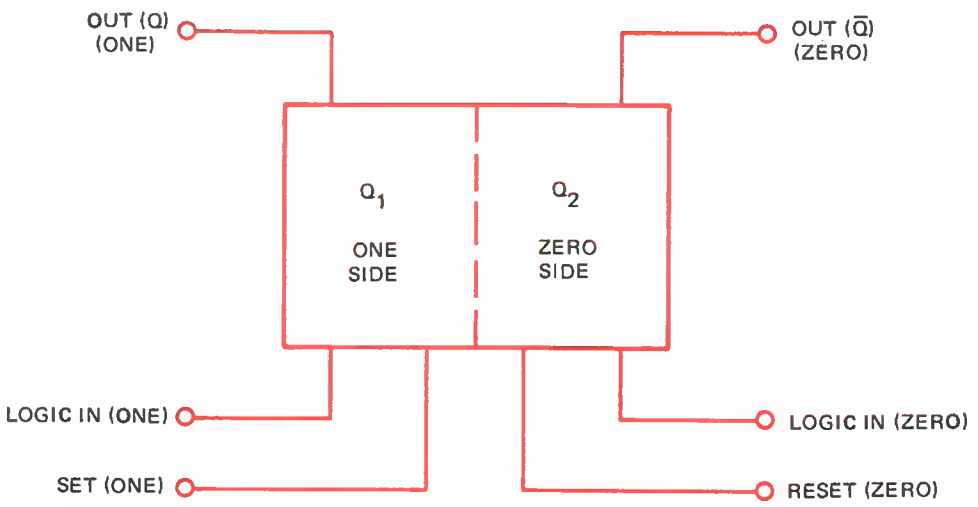


Fig. 16-5 Logic Symbol NPN Flip-Flop

Before we go further it is worthwhile to consider a particular triggering limitation of integrated circuits which is not always obvious to the casual observer.

Unlike basic DTL circuits, only the set and reset of the integrated circuit can be triggered by mechanical switching methods. When a mechanical switch is closed, it may actually open and close (bounce) several times in a fraction of a millisecond. Therefore, due to the sensitivity of the clock pulse, a triggering circuit is required which will not bounce in going from one state to the other.

The circuit which will be used in this experiment takes advantage of the ability to mechanically trigger the set and reset of an integrated circuit and therefore create a pulse of the desired type.

MATERIALS

2 Integrated circuits type SN15845 or equivalent
2 IC sockets
1 DC power supply (0–40V)
1 Oscilloscope
1 DPDT switch

PROCEDURE

1. Very carefully plug the IC into the socket. Observe the key mark as shown in figures 16-6 and 16-2.

2. Using figure 16-2 as a guide, hook up the power supply to provide V_{CC}. V_{CC} = 5V. **Do not turn the power on.**

3. Connect the DPDT switch so that a low input V(0) = 0V = ground may be applied to either the set or reset terminal when desired.

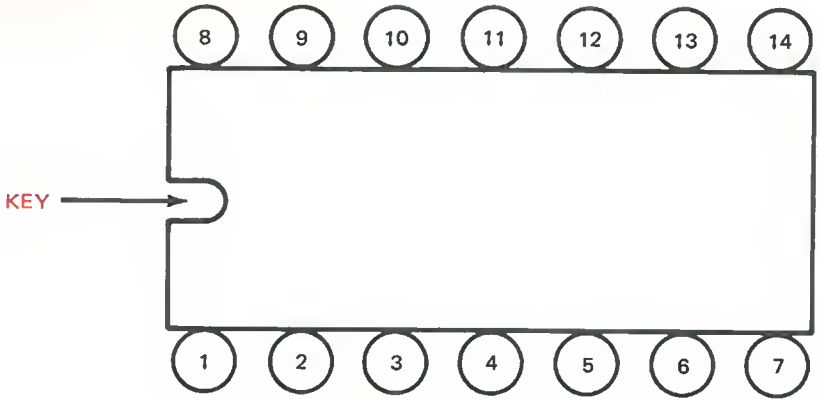


Fig. 16-6 The IC Socket

4. When you are sure the circuit and the polarity of the V_{CC} are right, turn on the power supply and record the output of this "triggering circuit" when a low input is applied to the set and reset terminal respectively. These ICs use positive logic. We now have a circuit which will supply the necessary pulse so that we can examine the different modes of operation of our ICs.

5. Turn the power off and connect a circuit so that the output, Q, of the "triggering circuit" is applied as the clock pulse of the other IC (leave the arm of the switch in a neutral position). The triggering circuit and the IC must have a common ground and V_{CC} = 5V.

6. Turn the power supply on and observe Q and $\overline{Q}$, the outputs of the IC (not the "triggering circuit"). If Q is in the 1 state (high state $\cong$ 5V) use the "triggering circuit" to change it to the 0 state.

7. Connect a "high" level input to S_1 and a "low" level input to C_1. Now, using the "triggering circuit", apply a pulse to the clock pulse input of the IC and observe Q and $\overline{Q}$.

8. Reverse the inputs of step 7 and apply another clock pulse while observing the outputs.

9. Fill in as much of the R-S Mode Truth Table, Figure 16-7, as possible at this time.

10. Repeat steps 6, 8 and 9 using inputs S_2 and C_2.

11. Short inputs S_1 to S_2 and C_1 to C_2 and repeat steps 7, 8 and 9.

12. Turn the power off and short terminals 4 to 9 and 11 to 6. The IC is now in the J-K mode.

13. Turn the power on and collect the data necessary to complete the J-K Mode Truth Table, Figure 16-7.

ANALYSIS GUIDE. The results of this experiment should be compared to the theoretical operation of a discrete flip-flop circuit. Discuss any difficulties that you encountered in carrying out the experiment.

R-S Mode Truth Table

t_n				t_{n+1}	
Inputs				Outputs	
S_1	S_2	C_1	C_2	Q	$\overline{Q}$
0	X	0	X		
0	X	1	X		
1	X	0	X		
X	0	X	0		
X	0	X	1		
X	1	X	0		
0	0	1	1		
1	1	0	0		
1	1	1	1	Indeterminate	

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

X = no input, terminal left floating

J-K Mode Truth Table

t_n		t_{n+1}
Inputs		Outputs
S_1	C_1	Q
0	0	
0	1	
1	0	
1	1	
X	X	

Triggering Circuit Data

Inputs		Outputs	
S_1	C_1	Q	$\overline{Q}$
X			
	X		
X			
	X		

Fig. 16-7 The Data Tables

PROBLEMS

1. What are the basic differences between PNP logic and NPN logic?
2. What would be the effect of clock pulses at the C_P input of the IC?
3. Would it be possible to *complement* the IC logic flip-flop? Explain.

INTRODUCTION. Multivibrators can be used as logic pulse generators as can a variety of other circuits. In this experiment we will investigate circuits for a self-gated pulse generator usually called a blocking oscillator. We will examine the design and waveforms for several basic types of blocking oscillators.

DISCUSSION. A *blocking oscillator* has the feature of being able to cut itself off after a prescribed period of conduction. In a blocking oscillator circuit, a transformer will normally be used to provide positive feedback from the output to the input of the circuit. Blocking oscillators may be either astable or monostable. The astable circuit is used as a source of pulses and as a generator of sawtooth waves. The monostable blocking oscillator is a favorite for development of logic pulses. Very fast rise and fall times with short pulse duration are readily obtainable. Like the Schmitt trigger, blocking oscillators are also useful in pulse shaping.

Figure 17-1 shows a basic astable common emitter blocking oscillator circuit. Notice the polarity markings on the transformer. These indicate connection so that a 180° phase shift occurs between the collector and the base. When the circuit is first energized, the only current flow in the collector circuit is the leakage. This leakage current I_{CO}, will induce a voltage in the base winding of the *transformer.* The base voltage (V_{BE}) will forward bias the base to emitter junction. Forward bias of the base-emitter junction will increase I_C, and I_C will increase V_{BE} some more. This increasing cycle will continue until a maximum amount of bias voltage is reached. This maximum will occur when the transformer or collector circuit are driven into saturation. That is, momentarily there will be no further change in the magnetic field around the collector winding of the

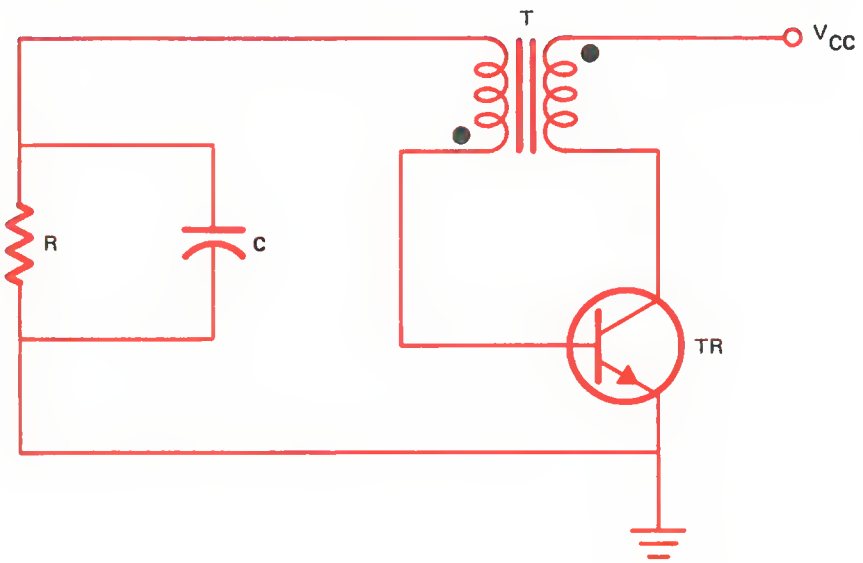


Fig. 17-1 Common Emitter Blocking Oscillator

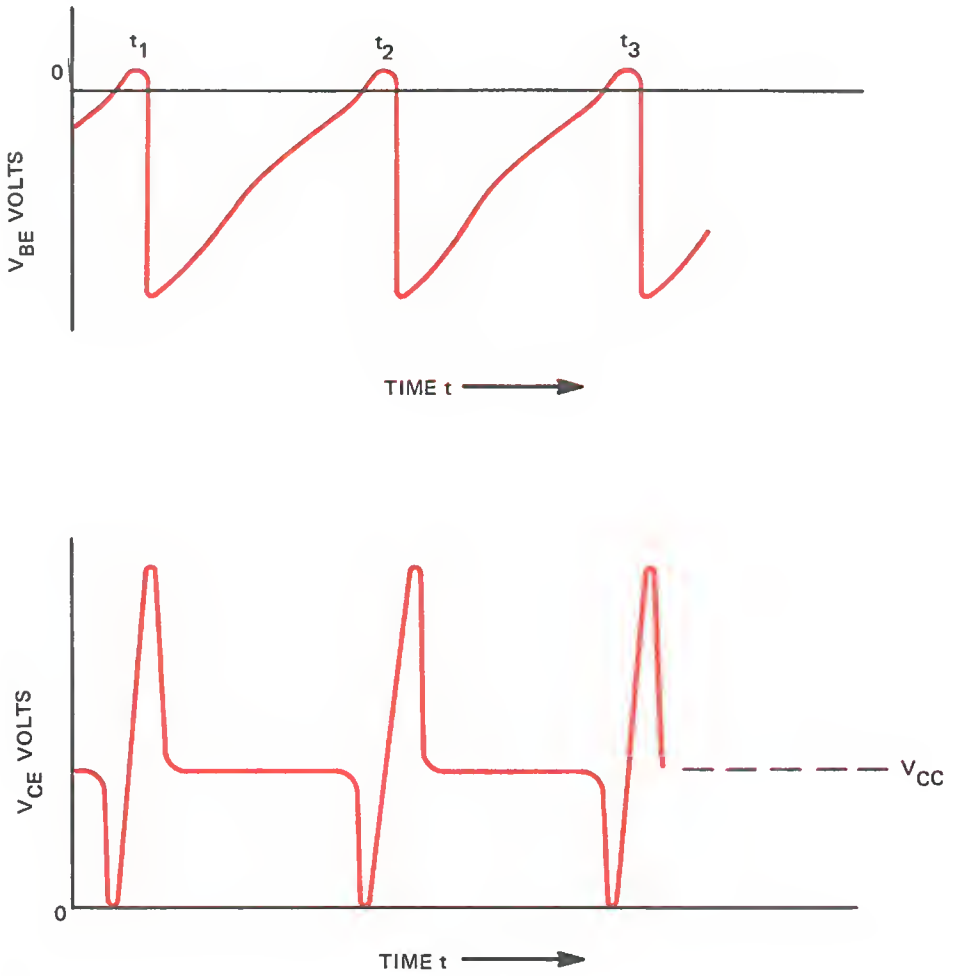


Fig. 17-2 Blocking Oscillator Base and Collector Voltage Waveforms

transformer. With no change in the flux at the collector winding, no voltage will be induced in the base winding; and the transistor will no longer be forward biased. Therefore, collector current drops. This drop in collector current causes a back EMF to develop in the collector winding inducing a reverse voltage in the base winding. These voltages will act to drive the transistor into cutoff.

While the transistor was conducting, the capacitor, C_1, was charged. When base current, I_B, stops, C_1 discharges until collector current can flow again. The cycle then repeats itself. Figure 17-2 shows the waveforms associated with the base and collector circuits during the oscillation cycle. Note carefully the relative phase relationship.

The instant the transistor is driven into cutoff, the collector voltage spike is much higher than the collector supply voltage. This is a function of the transformer winding, which acts as a voltage source that is attempting to maintain current (I_C) flow. The voltage at this point (V_{CE}) is the sum of V_{CC} and the EMF of the transformer winding. This represents a peak voltage which may

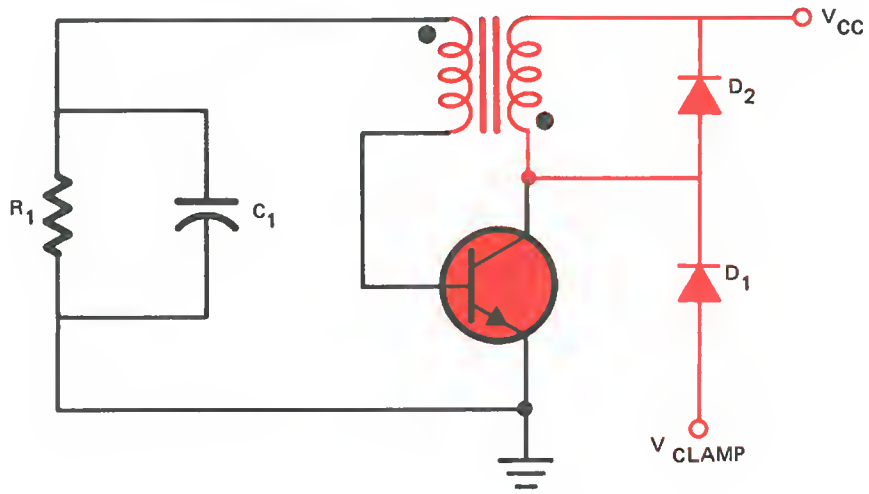


Fig. 17-3 Protected Blocking Oscillator Circuit

exceed the breakdown potential of the collector base junction. There is one other apparent fault with this basic circuit. The collector is purposely driven into saturation. This causes the circuit to suffer from the full effect of storage time delay and therefore sets the lower limit of pulse duration.

For these reasons, the basic circuit is usually modified to the circuit shown in figure 17-3. Diode D_1 is a voltage clamp which prevents the transistor collector from going deep into the saturation region. Diode D_2 is placed across the transformer winding to provide a path for the discharge of the voltage due to the magnetic field. This happens very quickly while the transistor is in cutoff. When the transistor is conducting, diode D_2 is reverse biased and has no effect upon the circuit. At the instant the transistor goes into cutoff, diode D_2 becomes forward biased and discharges the transformer winding at zero.

Often a third winding is provided on the transformer for coupling the actual output voltages. The major advantage of this type circuit is in its flexibility of design. The extra winding allows the addition of diodes across it for the limiting of both positive and negative excursions. The third winding is shown in figure 17-4.

Astable blocking oscillators may also be constructed using the common base configuration. This circuit is shown in figure 17-5. The circuit requires two voltage supplies. Voltage V_{EE} forward biases the emitter junction. Collector current flows and induces a voltage into the secondary and further increases the bias at the emitter. As in the previous circuit, saturation of the transformer core or transistor allows no further flux changes, and the induced voltage stops, removing the forward bias from the secondary. The capacitor, C_1, discharges the emitter to the base, reverse biasing the junction and driving the transistor into cutoff. The time required for the transistor in the cutoff region is equal to the time required for the capacitor to discharge.

With the voltage on C_1 at zero, the bias source V_{EE} will again forward bias the transistor and start a new cycle. The diode across the transformer prevents transistor breakdown.

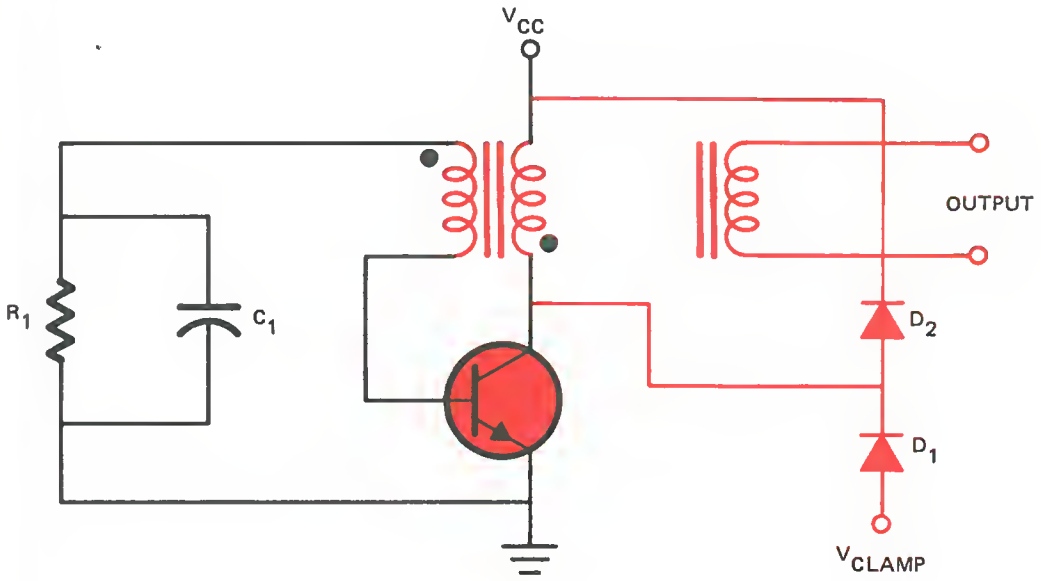


Fig. 17-4 A Common Emitter Blocking Oscillator with Transformer Coupled Output

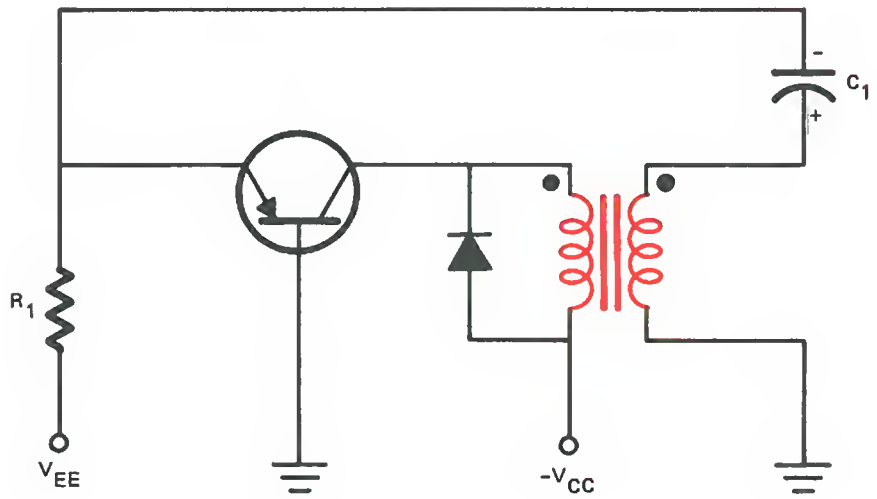


Fig. 17-5 Common Base Blocking Oscillator

Common base and common emitter forms of the blocking oscillator exist for the monostable version as well as for the astable. For both the monostable types, a reverse bias source must be used to keep the transistor in cutoff until a trigger pulse is applied. Upon application of the trigger pulse, the transistor conducts. Regenerative feedback increases the forward bias on the transistor until either the transistor or the transformer core saturates. Then the transistor will drop back to cutoff until the next trigger pulse is applied.

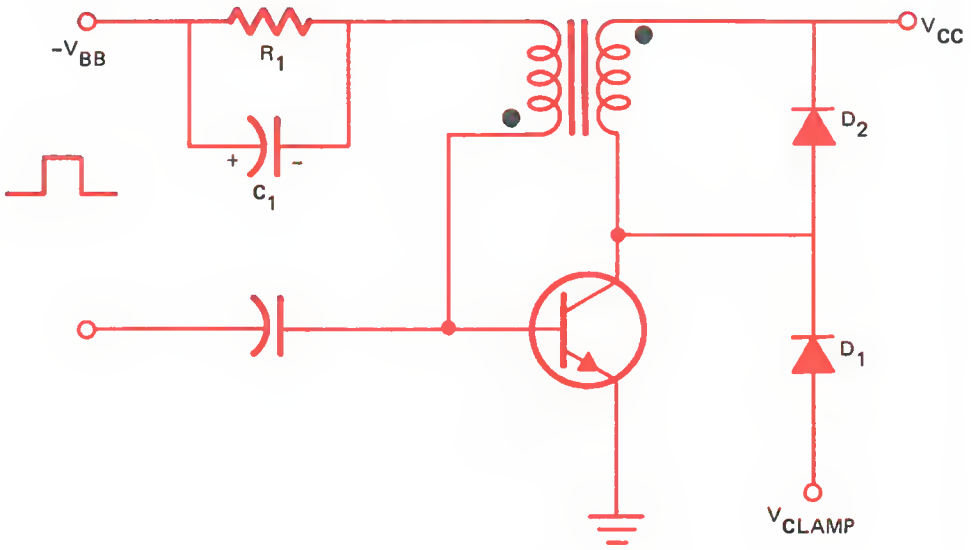


Fig. 17-6 Common Emitter Monostable Blocking Oscillator

Figure 17-6 shows the common emitter monostable blocking oscillator. For the stable state, the base-to-emitter voltage is $-V_{BB}$. Application of an input trigger causes collector current to flow and V_{CE} drops. Just as in the astable circuit, the transformer induces a base voltage of opposite polarity from the collector voltage. This drives the base positive and increases the collector current until D_1 conducts, limiting the voltage to a safe value when saturation occurs, and the magnetizing current of the collector becomes constant. No voltage is induced in the base winding. With the fall of collector current, the field around the collector winding begins to collapse, and this induces an opposite polarity voltage across the collector winding. This reverse pulse of voltage is induced into the base winding and drives the transistor into cutoff. D_2 discharges the collector winding and prevents breakdown.

When the transistor is in the active region (briefly), the bias developed across the base winding has to be greater than V_{BB}. The base current develops a charge across C_1. The actual reverse bias on the transistor at the instant of cutoff is given by

$$V_{\text{Reverse Bias}} = V_{BB} + V_{C_1} \qquad (17.1)$$

During the stable period, C_1 discharges through R_1. The base bias returns to $-V_{BB}$. The major limiting factor for maximum trigger rate is the time constant R_1C_1.

If V_{BB} is low, the amplitude of the trigger pulses can be small. A point is reached where the sensitivity is so great that the circuit will trigger on noise alone. Increasing the V_{BB} will make the circuit less likely to trigger on noise, but will also require a higher amplitude trigger pulse.

The common base monostable blocking oscillator is shown in figure 17-7. Positive trigger pulses cause collector current to flow through the transformer primary. This causes a forward bias on the emitter winding. An increase in collector current results with a corresponding increase in emitter current until the core of the transformer saturates.

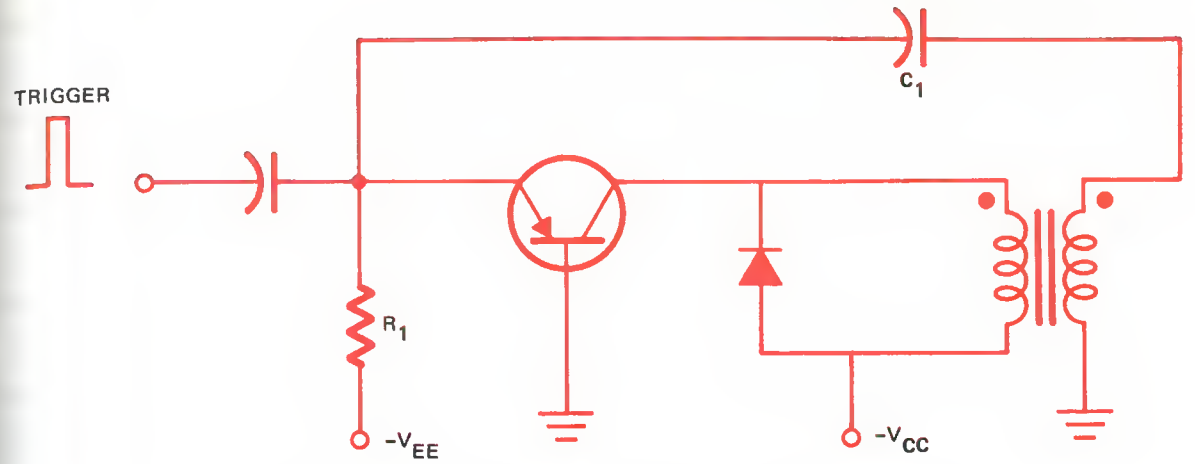


Fig. 17-7 Common Base Monostable Blocking Oscillator

When the core saturates, no feedback to the emitter is present and collector current starts dropping. The dropping collector current induces an EMF of opposite polarity across the primary. The decrease in magnetic field drives the emitter negative, and the transistor goes to cutoff. C_1 then discharges through R_1 and the transformer secondary. The two voltages (C_1 discharge and secondary EMF) are added and hold the transistor in cutoff. The trigger rate is limited by the R_1C_1 time constant and the secondary inductance (L).

The feedback requirements for this circuit are not so critical as they are for the common emitter circuit. The feedback loop is, in fact, paralleled by the reverse bias source $-V_{BB}$. The same sensitivity and stability conditions are appropriate for this circuit as were for the common emitter circuit.

MATERIALS

- 1 Transistor type 2N1304 or equivalent
- 1 Set of data sheets, 2N1304
- 1 Resistance substitution box (15Ω to 10 megΩ)
- 2 Capacitance substitution boxes
- 1 Function generator
- 2 DC power supplies (0–40V)
- 1 Oscilloscope
- 2 Semiconductor diodes (low forward drop)
- 1 Pulse transformer with 3 windings
- 1 Breadboard

PROCEDURE

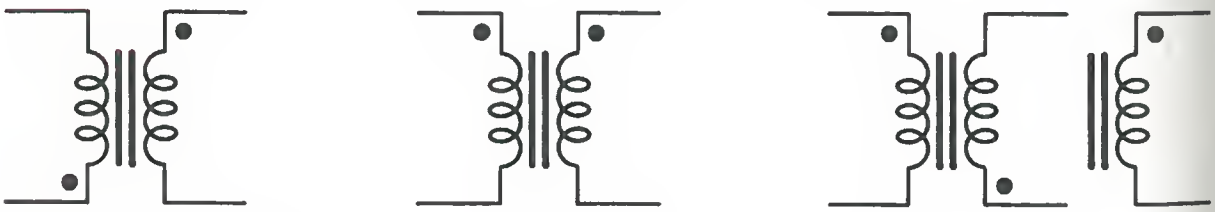
1. Determine the proper clamp voltage for the data sheet.
2. Assemble a circuit for the common emitter diode protected blocking oscillator, such as in figure 17-1.
3. Apply the proper clamping voltage at V_{CL}.
4. Apply the proper V_{CC} for oscillation (probably in the vicinity of 10V). Be sure to observe the proper polarity. R_1 and C_1 will require some adjustment. Start high. Record the values of R_1 and C_1.

5. Observe the V_{BE} waveform on the oscilloscope. Record its maximum and minimum values, frequency, and the rise time on a sketch of the waveform.
6. Observe the V_{CE} waveform on the oscilloscope. Record its maximum and minimum values, frequency, and rise time on a sketch of the waveform.
7. Vary the capacitor C_1 one step above and one step below the present value and record any changes in the V_{BE} and V_{CE} waveforms.
8. Disassemble the circuit and assemble a common base monostable blocking oscillator similar to figure 17-7.
9. Choose the proper bias ($-V_{EE}$) voltage to prevent transistor breakdown (see the data sheet) and a $-V_{CC}$ compatible with values of R_1 and C_1 for oscillation with a 3V input trigger pulse (low frequency).
10. Record the values of R_1' and C_1'. Record the maximum voltage, minimum voltage, frequency, and rise time on a sketch of the waveform of the output from collector to ground.
11. Vary the input pulse frequency and record the resulting change.
12. Vary the input pulse amplitude and record the effect.

ANALYSIS GUIDE. In analyzing these data, you should discuss the output waveforms of the two types of blocking oscillator. The effect of different values of R and C should be noted as well as the effects of varying the amplitude and frequency of the input pulses.

PROBLEMS

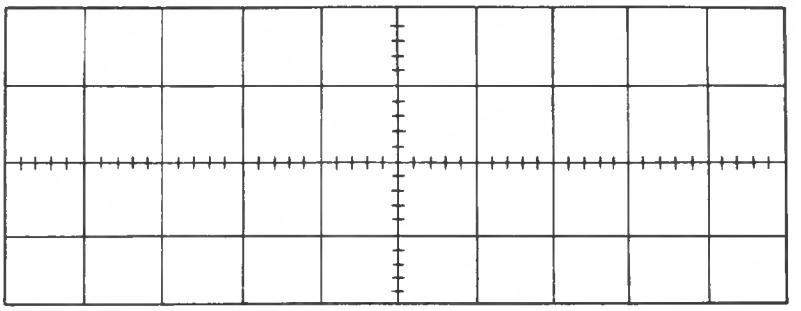
1. A common emitter blocking oscillator has a V_{CC} of 10V. The voltage induced across the transformer is 50V. What is the actual value of V_{CE}?
2. Determine the phase shift in the following transformers.



3. What is the effect of lowering the value of V_{BB} in a common emitter blocking oscillator?
4. List the components which determine the maximum trigger rate of a common emitter monostable blocking oscillator and of a common base monostable blocking oscillator.

R_1 = _____

C_1 = _____



Common Emitter V_{BE}

Effects of varying

R_1 _____

_____

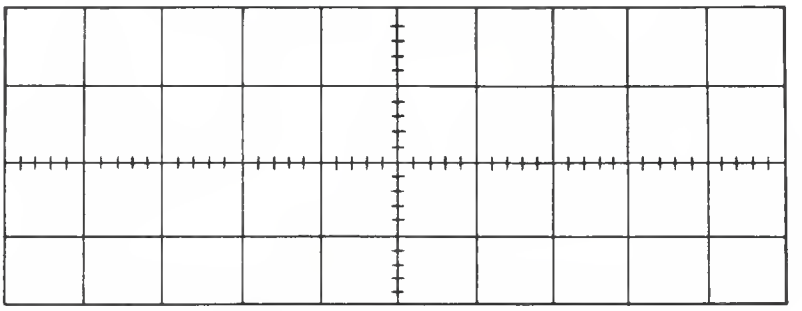
_____

Effects of varying

C_1 _____

_____

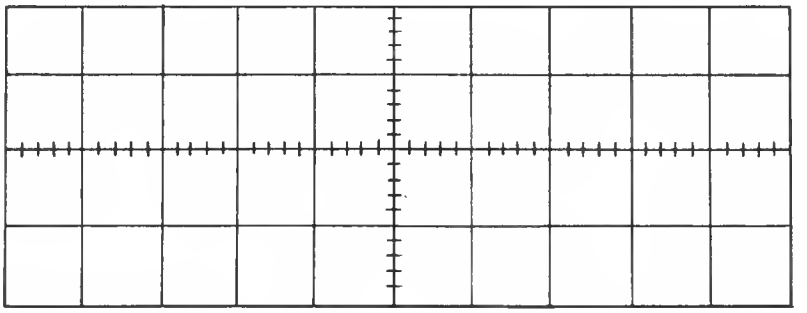
_____



Common Emitter V_{CE}

R_1' _____

C_1' _____



Common Emitter V_{CB}

Effect of varying trigger frequency _____

_____

Effect of varying trigger amplitude _____

_____

Fig. 17-8 The Data Tables

experiment 10010 TWO-DIODE STORAGE COUNTER

INTRODUCTION. As we deal with logic circuits and logic generators, it becomes apparent that some means must be devised to select and keep track of the pulses generated. One such storage circuit is the two-diode storage counter. In this experiment we will examine a simple staircase generator. We will look into the storage method and characteristics of this circuit.

DISCUSSION. Staircase generator is a name given to a two-diode counting circuit. This counting circuit has the ability to store the effect of pulses on its input and to trip at a predetermined count level.

For the present, let's disregard the voltage-operated discharge switch and consider only the counter itself. Refer to figure 18-1.

The output waveform for this circuit is shown in figure 18-2. The capacitor at the input allows us to assume a starting point for the voltage of zero volts. The initial charge on C_1 is zero as is the charge on C_2. When we apply an input pulse, the first one will cause C_1 to charge through D_1.

The rate at which C_1 will charge is determined by the RC time constant of C_1 and the sum of the diode resistance plus the generator resistance (around 500 kΩ for many generators). When this time constant is very small compared to the input pulse duration, the V_1 value will charge to the amplitude of the input pulse ($V_1 = E$).

While C_1 is charging, D_2 will not conduct and the voltage across C_2 will remain zero. After the pulse is past, C_1 is left with a charged voltage of $V_1 = E$ across D_1 and in series with D_2 and C_2. Because the polarity is reversed for D_1, it cannot conduct. C_1 wants to discharge, however, and does so through the source, D_2 and into C_2. C_2 will charge to equal the voltage at C_1 ($V_{C1} = V_{C2}$).

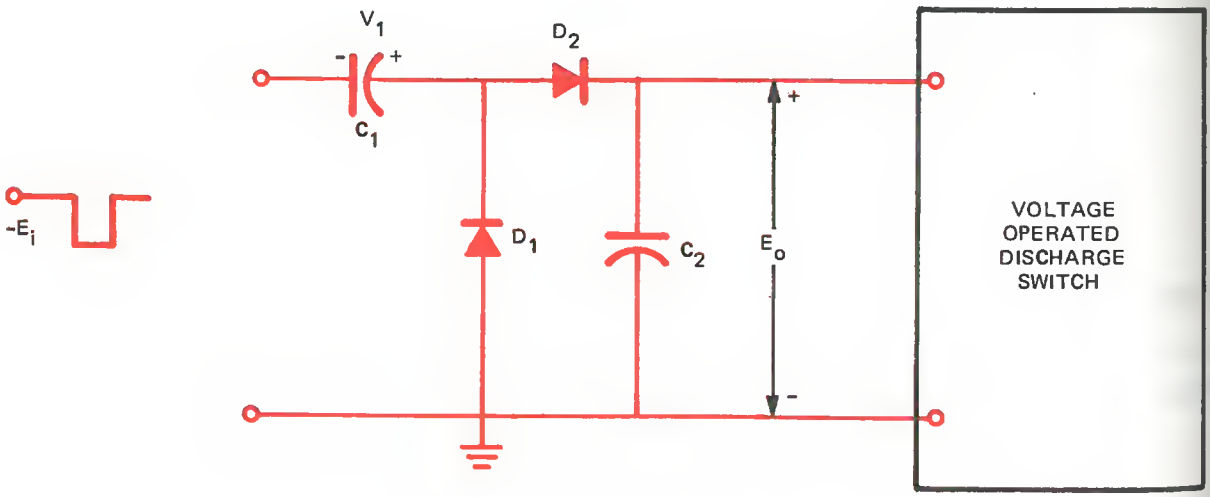


Fig. 18-1 Two-Diode Storage Counter

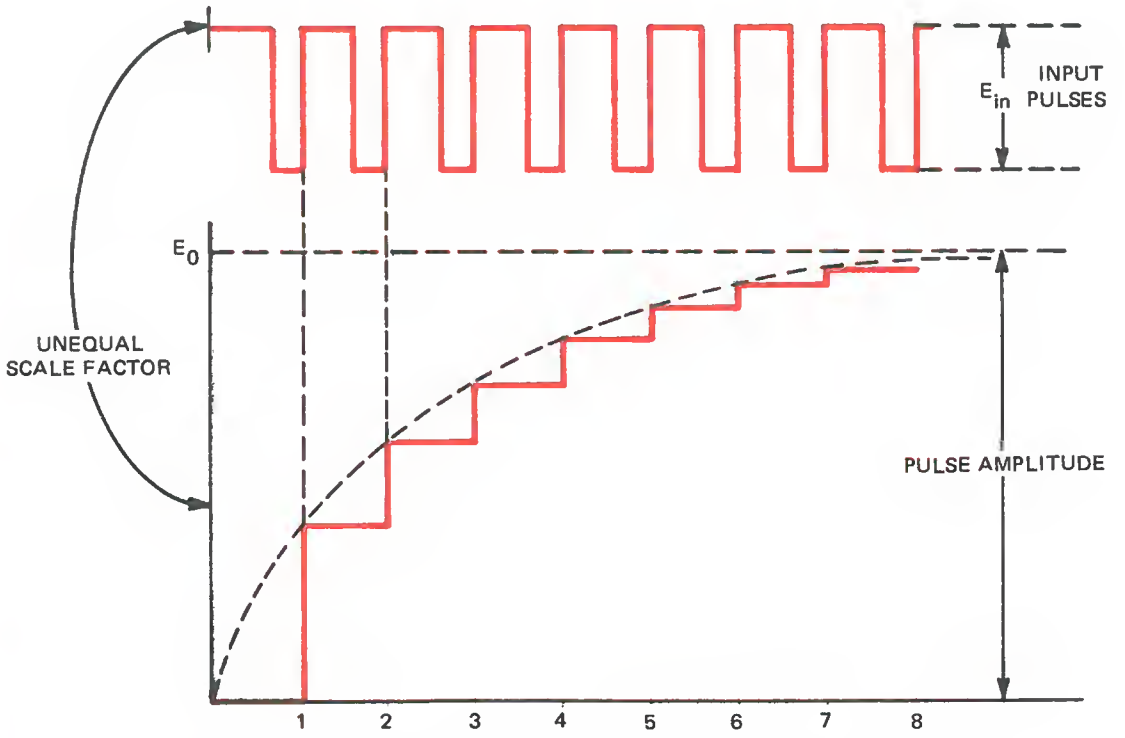


Fig. 18-2 Input Output Waveform Correlation Two-Diode Storage Counter

The time constant R_{D2} $(C_1 + C_2)$ must be quite small compared to the pulse off time in order for the voltages V_{C1} and V_{C2} to stabilize. For this reason, C_2 is ordinarily chosen quite large compared to C_1. Therefore, the *change* in voltage across C_2 will be small compared to V_{C1}.

During the time of the next input pulse, V_{C1} again charges to E and at the end of that pulse discharges into C_2. This stores a little more charge in C_2. Because C_2 has some initial charge from the first pulse, the amount of voltage transferred will be slightly less than was the case for the first pulse. Each successive input pulse will cause a progressively smaller voltage step at the output. The output, as shown in figure 18-2, will approach the value of the input pulse amplitude asymptotically.

To complete the counter, a circuit switch must be normally open. At some preestablished reference value (voltage level on C_2), the switch closes to give an output. As the charge leaves C_2, the switch will be reset to its original state ready for the next cycle.

A number of switches can be used for this purpose. Among them are *blocking oscillators, unijunction transistors,* and *neon bulbs.*

Let's examine what is possibly the simplest circuit and examine the staircase action. A neon bulb staircase generator is shown in figure 18-3. The bulb fires (conducts current) at about 70V. The input pulse must be greater than this because the maximum output is approximately equal to the pulse

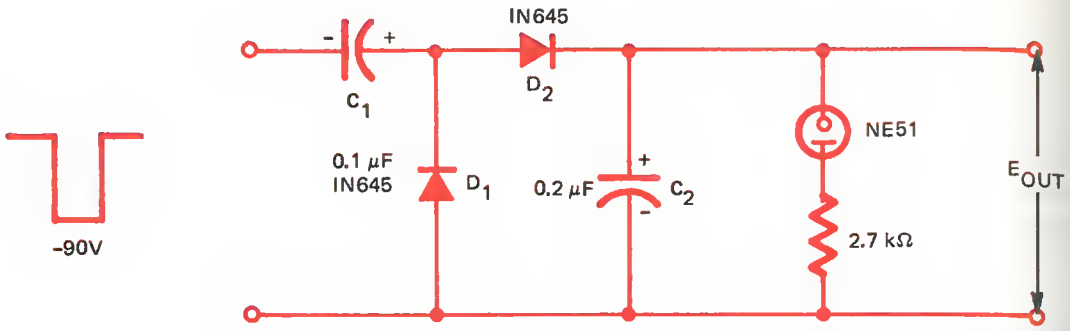


Fig. 18-3 A Neon Staircase Generator

amplitude. The circuit shown in figure 18-3 will give you about five steps with the bulb firing on the trailing edge of the sixth step. The action of the circuit is exactly as described before, with the 70V trigger point of the bulb setting the predetermined count level at C_2.

The number of steps may be increased by increasing the capacity of C_2. Decreasing the capacity of C_2 will decrease the number of steps. The counting ratio may be increased by raising the voltage at which the comparator (bulb) responds. A maximum practical value is soon reached, however, because the reliability of the level across C_2 becomes uncertain as the steps approach closer and closer to the pulse amplitude E. The difference voltages per step become so small that noise and fluctuations in the voltage obscure the action. Normally, the maximum practical number of steps for one stage of storage is about ten. Because of this decrease in step size with the number of steps, counters may be cascaded to obtain more steps.

We can write equations for the number and size of the steps. The equivalent circuit in figure 18-4 will be helpful in understanding the mathematics. This circuit represents the circuit state when diode D_2 is conducting, as represented by S. Writing the equation for the voltage across C_2 at the first step (V_{n+1}), we have

$$V_{n+1} = V_n + (V - V_n)\frac{C_1}{C_1 + C_2} \qquad (18.1)$$

where n is the number of the step.

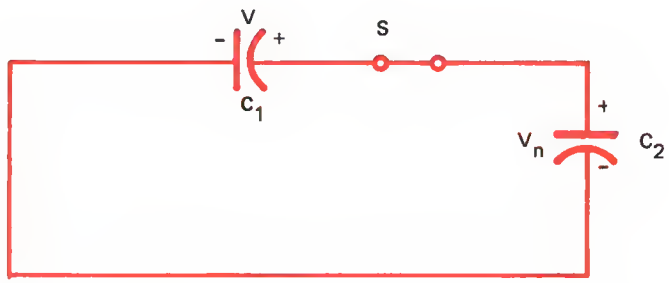


Fig. 18-4 Equivalent Circuit for Calculating Step Voltage

Since the change in $V_n - V$ $[\Delta(V_n - V)]$ is proportional to $V_n - V$, then it will vary exponentially with n as seen in figure 18-2. Thus, the exponential charge relationship is

$$V_n - V = A\epsilon^{\alpha n} \qquad (18.2)$$

where A and α are circuit constants determined by the characteristics of the actual components involved.

$$V_n - V_{n+1} = \left(\frac{C_2}{C_1 + C_2}\right)(V_n - V) \qquad (18.3)$$

Substituting equation 18.2 into equation 18.3, we have

$$A\epsilon^{\alpha(n+1)} = \left(\frac{C_2}{C_1 + C_2}\right) A\epsilon^{\alpha n} \qquad (18.4)$$

which renders

$$\epsilon^{\alpha} = \frac{C_2}{C_1 + C_2} \qquad (18.5)$$

or

$$V_n - V = A\left(\frac{C_2}{C_1 + C_2}\right)n \qquad (18.6)$$

So

$$V_n = V + A\left(\frac{C_2}{C_1 + C_2}\right)n \qquad (18.7)$$

Now, for $n = 0$, V_n = some voltage V_1, and A is defined as

$$A = V_1 - V \qquad (18.8)$$

Therefore, the voltage for each step (V_n) can be calculated using

$$V_n = V - (V - V_1)\frac{C_2}{C_1 + C_2} \qquad (18.9)$$

The total difference in level between the n step and the n + 1 step is

$$V_{n+1} - V_n = (V - V_1)\left(1 - \frac{C_2}{C_1 + C_2}\right) - \left(\frac{C_2}{C_1 + C_2}\right)n \qquad (18.10)$$

An example might help. Suppose that

$V = 110V$

$V_1 = 10V$

C_2 is 9 times larger than C_1

$$V - V_1 = (110 - 10) = 100V$$

but

$$C_2 = 9C_1 \text{ or } \frac{C_2}{C_1 + C_2} = \frac{9}{10}$$

So

$$(100)\left(1 - \frac{9}{10}\right) = 10V \qquad (18.11)$$

The first step has a level of 10V. The tenth step has a level of:

$$100\left(1 - \frac{9}{10}\right) - \left(\frac{9}{10}\right)10 = 1V \qquad (18.12)$$

Storage counters are limited to counting pulses which are all the same. This is true

because the step level (and dependability) is determined by the charge on C_2. This charge will leak off through the load no matter what type device is used as a discharge switch. The capacitor must be able to charge quite rapidly, and this means its size must be relatively small. Where storage counters can be used, they are much cheaper then binary counters.

The counter may be used with positive input pulses with C_1 charging first through D_2 and thereafter through D_1. One difference is that the step at C_2 will occur at the leading edge of the input pulse. The counter may be operated with either polarity of input pulse by reversing the polarity of the diodes. When this is done, the output steps will also be reversed.

MATERIALS

- 2 Capacitor substitution boxes
- 2 Resistance substitution boxes (15Ω - 10 meg)
- 4 Diodes type 1N34 or equivalent
- 1 Function generator
- 2 Neon bulbs w/socket type NE51 or equivalent
- 1 Oscilloscope
- 1 Breadboard

PROCEDURE

1. Connect a circuit similar to the one shown in figure 18-3.
2. Apply 45V negative pulses of appropriate duration at a rate of about 100 Hz.
3. Observe the output on the oscilloscope.
4. Record the number of steps and sketch the waveform. (each cycle)
5. Measure the amplitude of each step and record the results on your sketch.
6. Calculate the amplitude of each step using the circuit values measured in equation 18.9.
7. Observe the output across the 2.2 kΩ resistor, and record the waveform and its values. (Don't forget the frequency.)
8. Decrease the value of C_1 and increase the value of C_2 by two steps on the substitution boxes.
9. Repeat steps 2 through 7.
10. Reverse the polarity of the input pulse.
11. Record the effect using a sketched output waveform.
12. Reverse the neon bulb. Record the effect.
13. Assemble a second circuit similar to figure 18-5, and restore the original to the circuit values of figure 18-3. Take the output of the first and feed it into the input of the second. (See fig. 18-5). Use positive input pulses to #1 staircase.
14. Observe output one and output two. Record both waveforms.

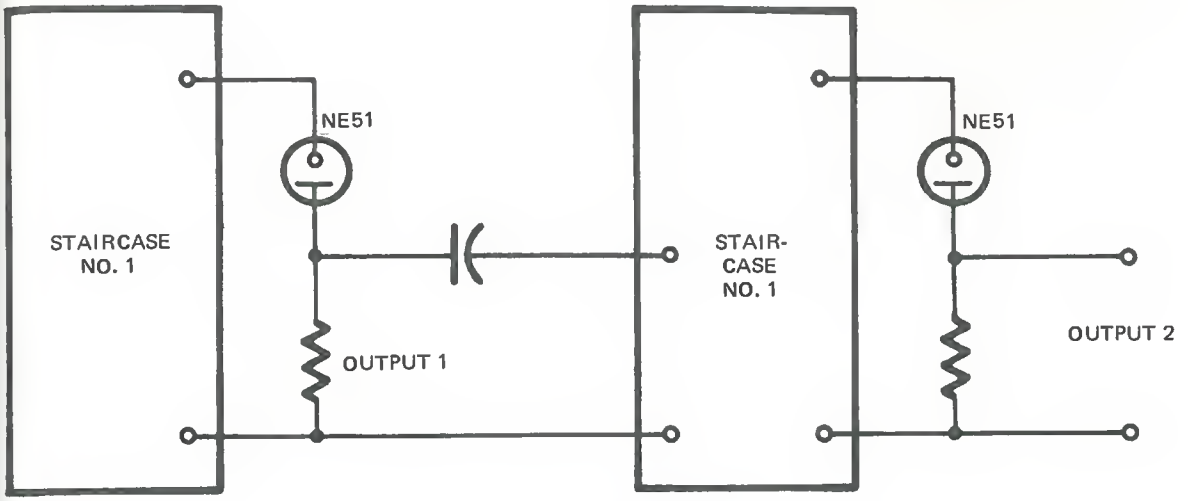


Fig. 18-5 The Second Experimental Circuit

ANALYSIS GUIDE. In analyzing these data and waveforms, you should comment on the important characteristics of the two-diode storage counter and its operation. Discuss how the two waveforms in step 14 compare to each other.

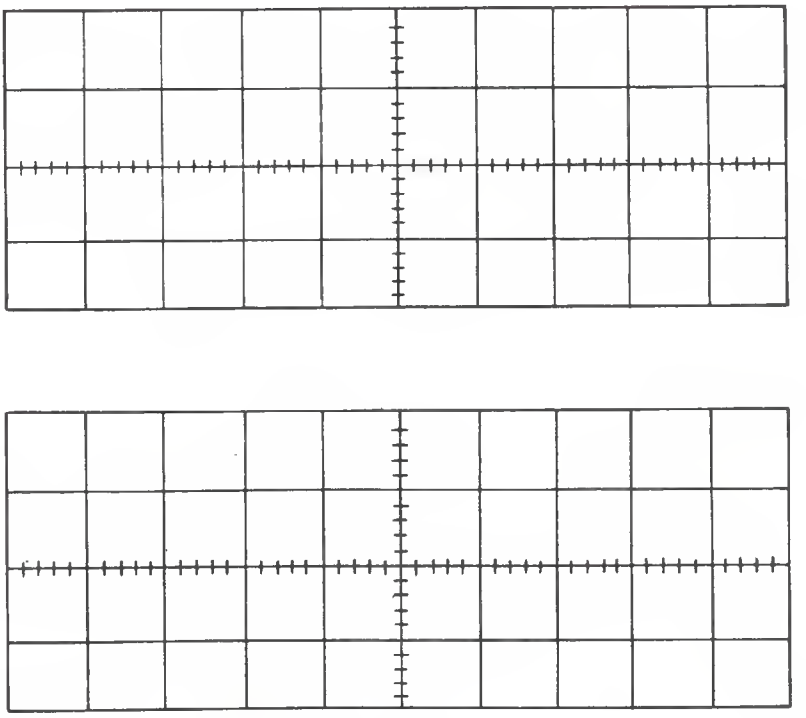


Fig. 18-6 The Results

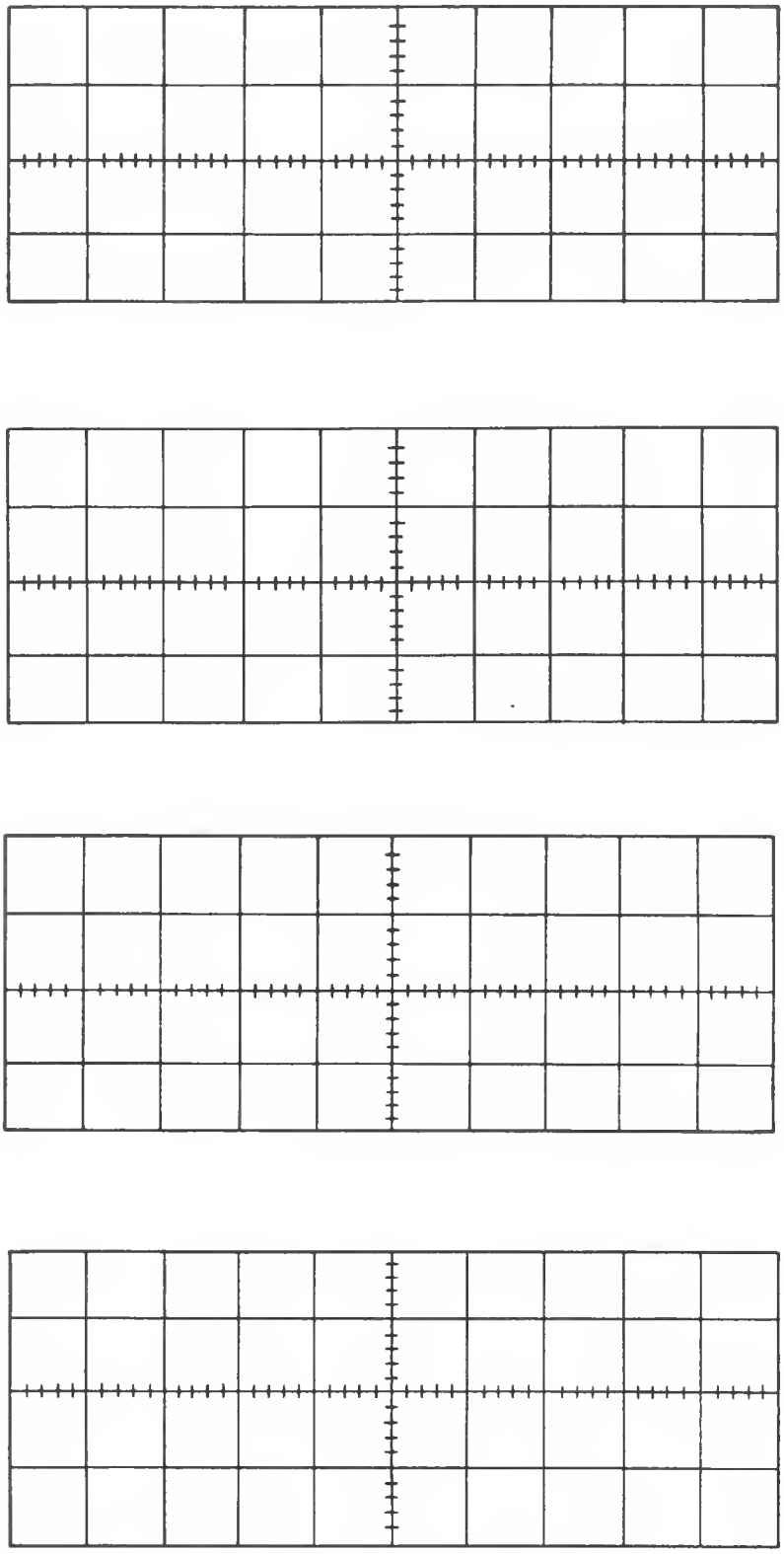


Fig. 18-6 The Results (Cont'd)

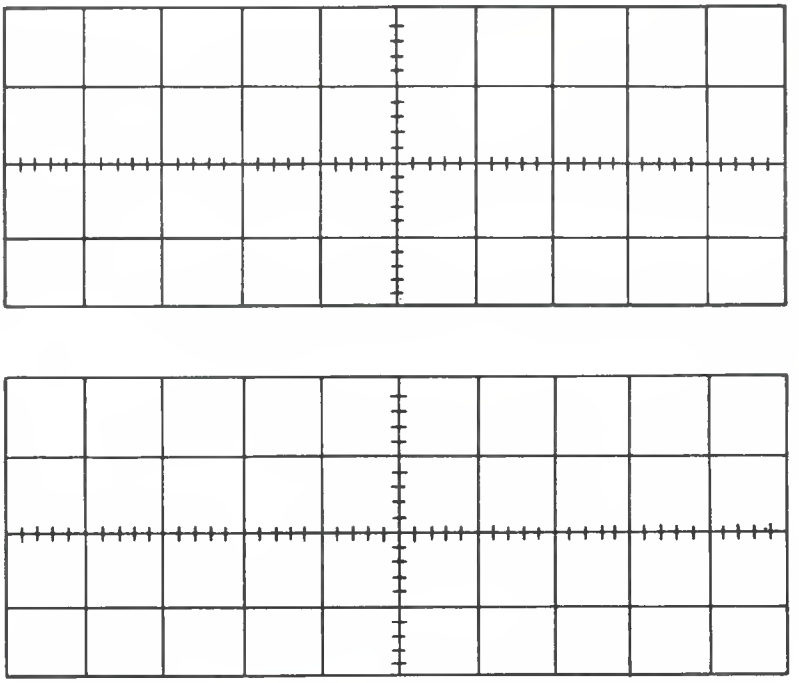


Fig. 18-6 The Results (Cont'd)

PROBLEMS

1. A certain staircase generator generates six steps. It is feeding three other two-diode storage counters which generate three, five, and four steps, respectively. How many pulses will be required on the input of number one to get one pulse out at number four?

2. $C_1 = 0.01\mu F$

   $C_2 = 0.02\mu F$

   A. What is ΔV_{C2} for step one?

   B. Step six?

3. It is desired to have a storage counter that will trigger on every twelve input pulses. Sketch the circuit you would use. Any type of trigger device (discharge switch) may be used.

experiment 10011 BASIC COUNTERS

INTRODUCTION. Multivibrators are used extensively throughout logic circuitry. The bistable multivibrator, in either the saturating or nonsaturating configuration, is especially useful in logical counting applications. In this experiment we are going to investigate the use of a bistable multivibrator with binary coded numbers.

DISCUSSION. The bistable multivibrator circuit has two stable states. This makes it especially useful in the binary coded number system. Both the saturated and the nonsaturated versions are used. The saturated types have the advantage of being easier to design and build. They require fewer power supplies and, in the long run, are more reliable and have less susceptibility to noise. Saturation, however, causes the switch action to be slower, due to the collection of charges in the transistor while it is operating in the saturation region. The slow switching action of saturated flip-flops makes them particularly useful in industrial circuits which do not require high-speed switch action and rapid calculations.

The nonsaturated type has the advantage of very high-speed switching at the cost of more complicated circuitry. These are the type most often used in digital computers. They overcome the storage delay time required by the saturated transistor.

The multivibrators of any counter must have symmetrical triggering for advancing the count, and nonsymmetrical triggering to allow the circuit to be reset. The number of flip-flops in the counter is determined by the size of the numbers to be handled. This can be calculated using

$$N = \frac{\text{Log}_{10} Y}{0.301} \qquad (19.1)$$

where

N is the number of bistables.

Y is the decimal number to be counted.

Another equation with the same prediction stated differently is

$$\text{Maximum count} = 2^N - 1 \qquad (19.2)$$

where N is still the number of flip-flops. Thus, a four-flip-flop counter can count a maximum of 15. Figure 19-1 shows such a four-stage binary counter. The input pulses are fed to the first J-K flip-flop (FF_0). The reset pulses can be fed to all of the FFs at the same time, or the J-K operation can automatically set them. The circuit blocks (flip-flops) represent the powers of two in the binary number system.

$$FF_0 = 2^0$$
$$FF_1 = 2^1$$
$$FF_2 = 2^2$$
$$FF_3 = 2^3$$

It is very easy to determine that $2^0 + 2^1 + 2^3 = 15$.

When the first bistable (FF_0) switches from 0 to 1, the second bistable (FF_1) will not switch because the pulse is inappropriate to switch FF_1. When FF_0 switches from 1 to 0, then FF_1 will receive a pulse which will

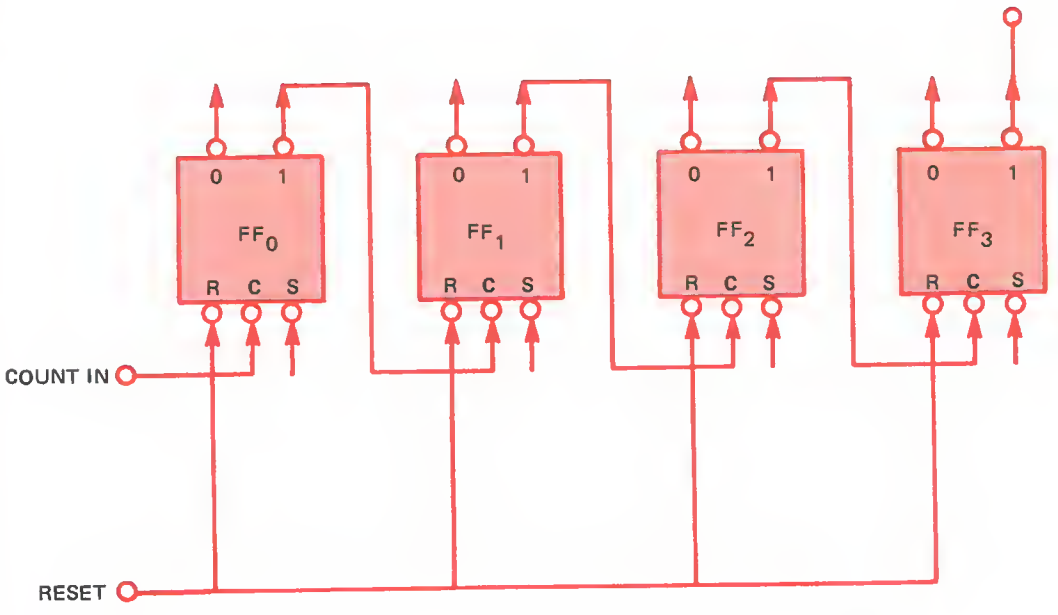


Fig. 19-1 Four-Stage Binary Counter (All FFs in J-K Mode)

switch it from 0 to 1. Thus, two pulses into FF_0 will cause FF_1 to switch and produce a pulse. This pulse will not switch FF_2 because, like FF_1, it must receive the appropriate pulse polarity, which will be passed only when FF_0 receives enough pulses to change FF_1 back to its original state.

So we see, in like manner, any number of flip-flops can be linked to produce any desired decimal-binary conversion. It is true that a bistable multivibrator can be made to respond to either positive or negative pulses.

What happens electronically? When the multivibrator is in the zero state, the output transistor is in saturation. Application of the correct pulse polarity to the input will cause the output transistor to go into cutoff (and the input transistor to saturate). At that instant the change in voltage at the output collector (negative with PNP transistors and positive with NPN transistors) is coupled to the input of the next bistable. By proper arrangement (similar flip-flops), this pulse will be of the wrong polarity to switch the next flip-flop. When two pulses are received at the input of the bistable, the output will first go to cutoff, then back to saturation. As the transistor switches from cutoff back to saturation, a pulse of the correct polarity to switch the next FF will be coupled from the output collector. This pulse acts just like the first pulse did on the original FF, and so on down the chain.

We will assume that the transistors in the example are PNP. The magnitude and polarity of the voltage at the collector is from near 0 to $-V_{CC}$ with the first switch (0 to 1), and $-V_{CC}$ to near 0 when it switches from 1 to 0. A PNP bistable circuit is usually triggered with positive pulses, and this will happen at the collector when V_{CE} changes from $-V_{CC}$ to near 0. This condition is shown in figure 19-2. The counter is said to be *full* at the 15th

pulse, and all bistables are reset by the 16th pulse. The truth table for this counter appears in figure 19-3. This table is useful in revealing the actual state of each FF and, therefore, the number of pulses which have been fed to the input of the counter. Notice also that the state of the FF corresponds to the binary number for each decimal count.

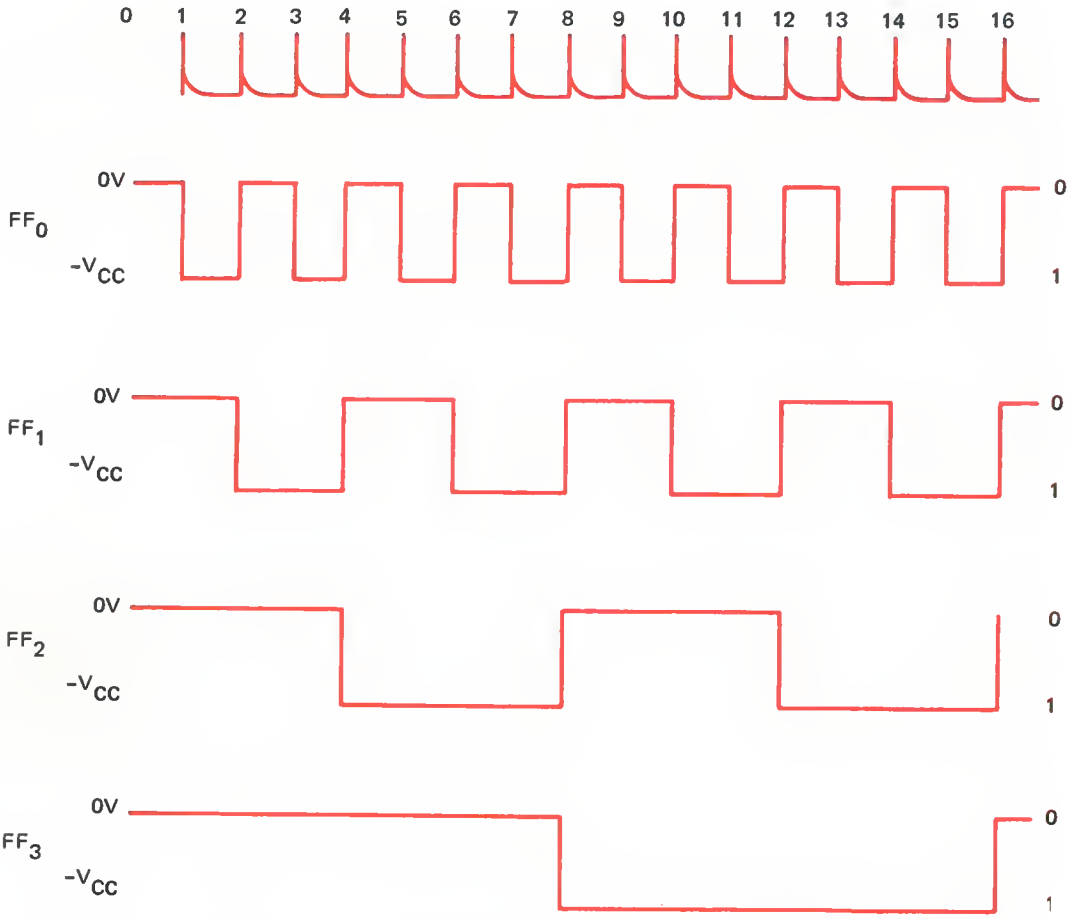


Fig. 19-2 Voltage Waveforms of a Four-Stage Binary Counter (The FFs used above trigger on positive-going pulses)

Count (or pulse)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FF_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
FF_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
FF_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
FF_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0

Fig. 19-3 Truth Table for Four-Stage Binary Counter

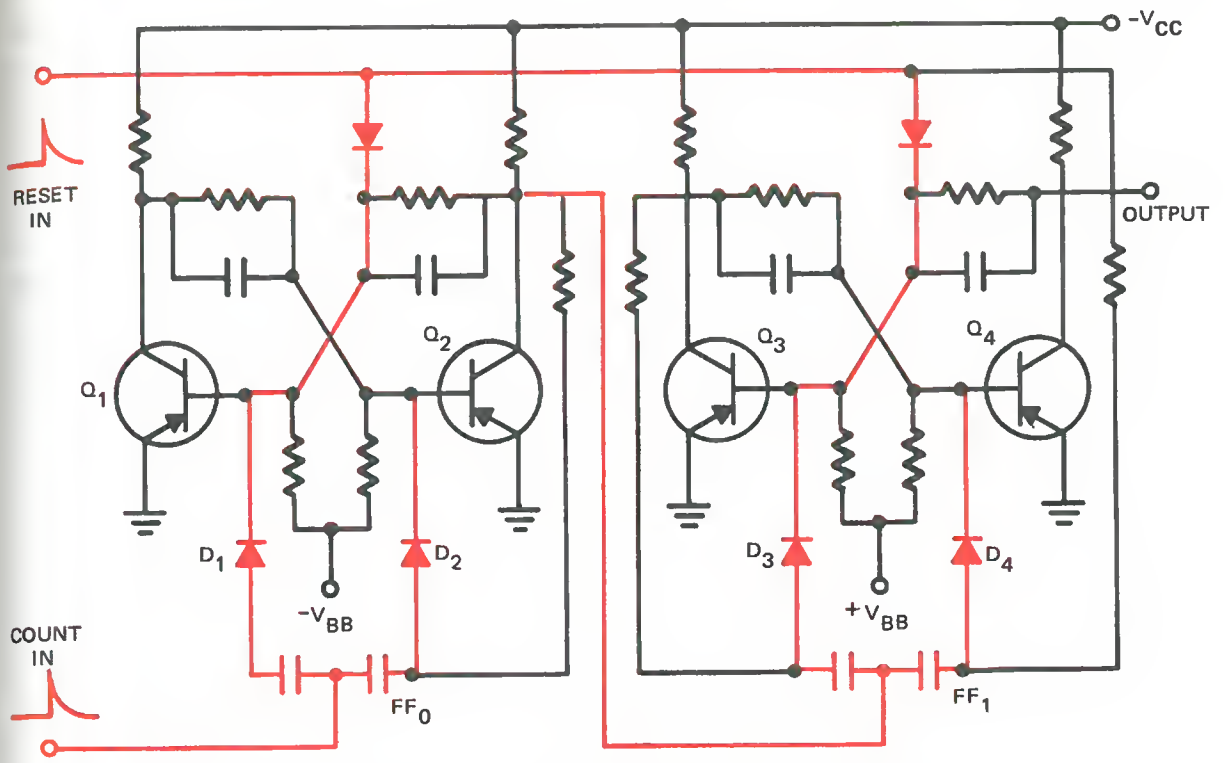


Fig. 19-4 Two Stages of Diode-Steered Base-Triggered Binary

Probably the most important consideration for designing a counter after choosing the FFs is the manner in which they are to be coupled. Figure 19-4 shows the circuit for a bistable pair with diode steering and base triggering. The diodes are so placed that they make the multivibrators respond only to positive pulses, and the reset line will switch both output transistors to the saturated state. To do this, the input transistors are supplied a positive pulse to turn them off.

When a reset pulse is applied, Q_1 and Q_3 are driven into cutoff. Q_2 and Q_4 will conduct at the saturation level. A count pulse is directed to Q_2 by D_2, and Q_2 will cut off, throwing Q1 into saturation. This will cause a negative pulse to go to FF_1 which will *not* appear at the base of Q_3 or Q_4 because of the diode (D_3 and D_4) steering circuits. Consequently, this bistable does not change its state.

When the next count pulse is applied to FF_0, it does change its state; Q_1 cuts off and Q_2 goes to saturation. The output at the collector of Q_2 now pulses from $-V_{CC}$ to near 0 (a positive pulse). This positive pulse is coupled to the input of FF_1, and the diodes direct it to the bases of Q_3 and Q_4. Since Q_3 is already cutoff, nothing happens at its base. But the pulse at the base of Q_4 will cause it to cut off. When Q_4 cuts off, Q_3 must go to saturation. Again, a negative pulse occurs at the output. This will go to the next stage (not shown) where the steering diodes will block it. The pulse count is 2, and the binary reads 10. The third pulse (count 3) switches FF_0 to the 1 state. The resulting negative pulse will not switch FF_1, and it will remain at 1. The binary count now becomes 11. This is carried out through all stages until the maximum capability is reached, and then all are returned to 0 by the first count beyond its maximum count.

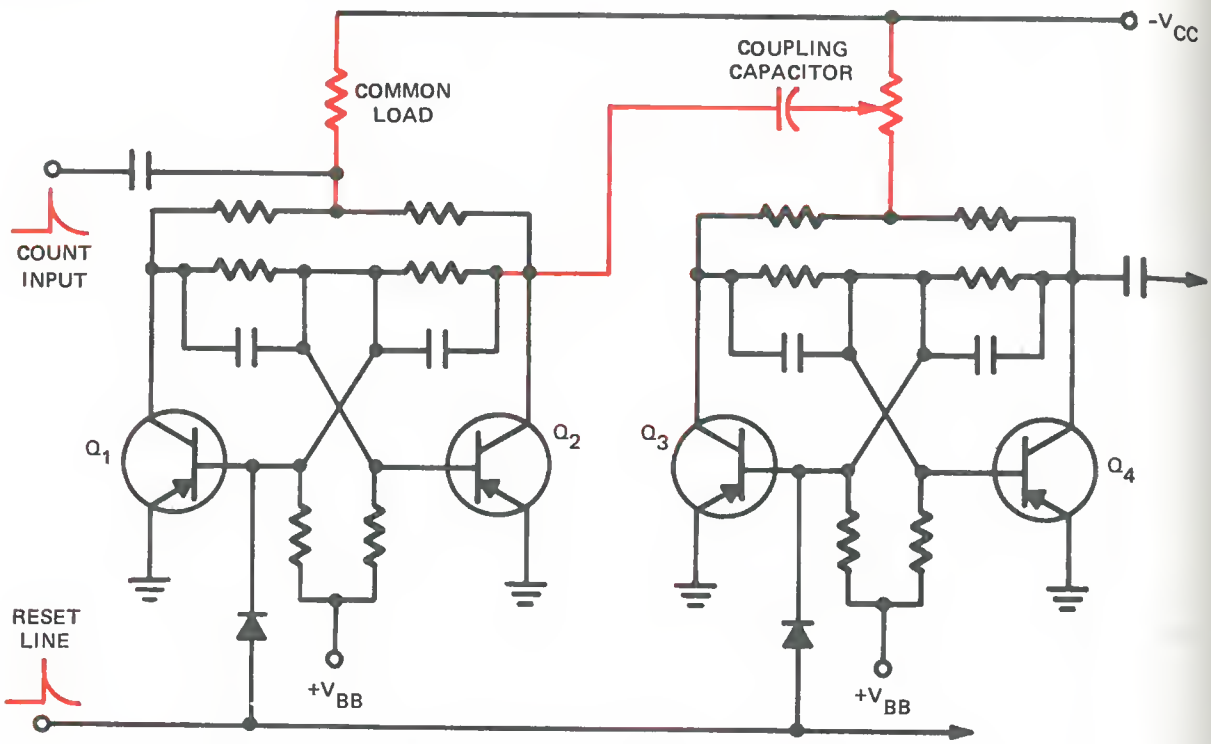


Fig. 19-5 Binary with Common Load Resistor and Capacitor Coupling

A common load resistor and single coupling capacitor can be used as shown in figure 19-5. There is still no problem with a negative pulse switching the FF, but a positive pulse from the first stage to the second will tend to turn the ON transistor of the second FF off.

When a high speed counter is desired, the bistable circuits must be of the nonsaturating type. Collector triggering is often used for faster switching response, and to minimize the load on the pulse source. Clamping is used to prevent saturation of the collector circuit. Actual circuit operation is very similar to that already discussed. Any counter can be speeded up by using AND gates to sense the bistable states. This type of circuit is shown in figure 19-6. Such an arrangement eliminates the time delay required for each bistable to switch in sequence. The AND gates direct the pulses to the proper flip-flop.

The input count pulse is applied to the first FF and to the first AND gate. If the FF is in the zero state, no output will go to the next stage because the required second pulse to the AND circuit will be missing. The FF will shift from zero to one. When the second pulse is applied, the AND gate will produce an output one because both of the inputs to it are 1s (if necessary, refer to the truth table for AND gates clarification). The counting proceeds as in the previous circuits. The increased speed is the only real difference in the counter operation. This also creates a major problem with the gated counters. There is a possibility for a bistable to switch states before the AND gate, on its output, can sense its change. In this case, a delay must be inserted between the one output and the AND gate input to slow the shift indication. The delay is normally only a few microseconds, and the counter will still operate faster than the ordinary type.

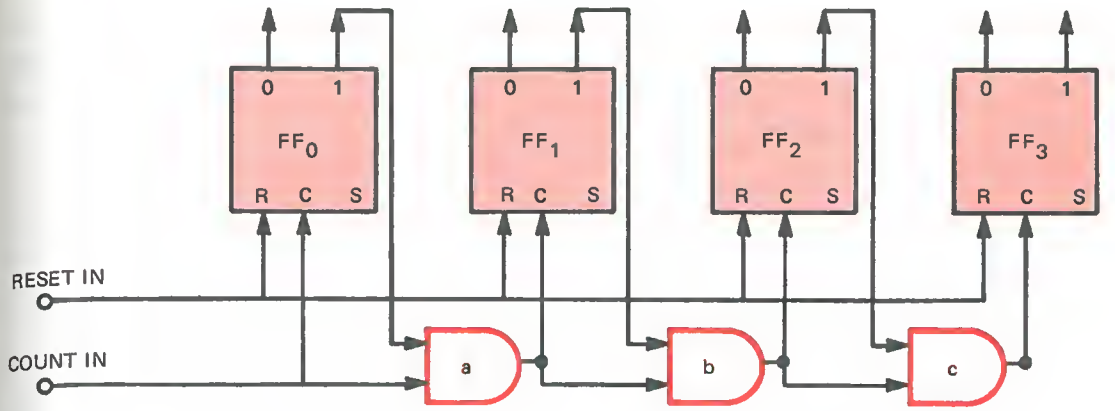


Fig. 19-6 Gated Binary (All FFs in J-K Mode)

MATERIALS

- 4 Integrated flip flops, type SN1584N or equivalent
- 1 Data sheet for the IC FF
- 1 DC power supply (0 - 40V)
- 4 IC sockets appropriate for the ICs
- 1 Oscilloscope
- 1 Function generator
- 1 DPDT switch
- 1 SPST momentarily-closed switch

PROCEDURE

1. Determine the correct number of FFs for a maximum count of seven. Show all of your work.
2. Draw a block diagram similar to figure 19-1 of a circuit using IC flip-flops in the J-K mode for a maximum count of seven. Show your block diagram with a coupling reset switch (SPST) and supply voltages. **Have the instructor check the drawing before proceeding.**
3. Checking figure 19-7 and being very careful to plug in the IC correctly, construct your circuit. **Remember, these ICs use positive logic.**

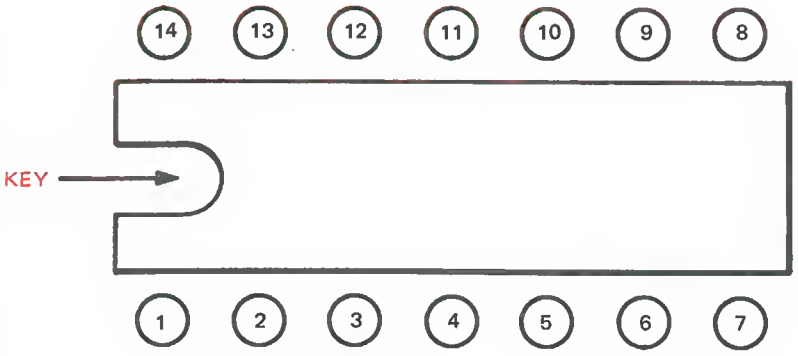


Fig. 19-7 The IC Socket

4. Connect a "triggering circuit" using a V_{CC} of 5V and a DPDT switch to short either the set or reset terminal of one IC to ground. The output of this "triggering circuit" should be applied to the clock pulse terminal of FF_0. The counting circuit and triggering circuit must have a common ground and V_{CC} = 5V.
5. Check the data sheet for the proper V_{CC} (magnitude *and* polarity). **Be sure to monitor this voltage constantly with an accurate meter. It cannot vary more than 1.5V without destroying the IC.**
6. Check the terminals for accidental short circuits. **These can easily destroy an IC.**
7. Apply V_{CC} to the whole system.
8. Observe the outputs (Q) of FF_0, FF_1, and FF_2. If they are not *all* in the 0 state, use the SPST switch to momentarily ground pin 5 (C_D) of all the FFs. Recheck the outputs to see if they are now all in the 0 state.
9. Now use the "triggering circuit" to apply pulses to the binary counter and complete the data table.
10. Observe what happens if the reset switch is closed while the counter is in a state other than 000.
11. Turn the power supply off and disconnect the triggering circuit from the binary counting circuit.
12. Now connect the function generator (pulse output) with the amplitude off to the clock pulse of FF_0.
13. Turn the power supply back on, set to V_{CC} = 5V. Now adjust the function generator so that a pulse train of about 7 positive, 4-1/2V pulses being applied to the clock pulse input of FF_0 can be seen on the oscilloscope. Set the oscilloscope triggering for negative internal trigger slope.
14. Now make *accurate* sketches of the pulse train being applied to FF_0 and the output of FF_0, FF_1, and FF_2 in the space provided on the data table.
15. Observe the outputs when the reset switch is momentarily closed.
16. For your own understanding, observe the outputs when pulse trains of different frequency and duration are applied to the counter. **Do not exceed 4-1/2 volt pulses in amplitude as this may destroy the IC.**

ANALYSIS GUIDE. In analyzing these results, you should describe the operation of the bistable multivibrator as a basic binary counter. Also discuss any problems you had in getting the system to work properly.

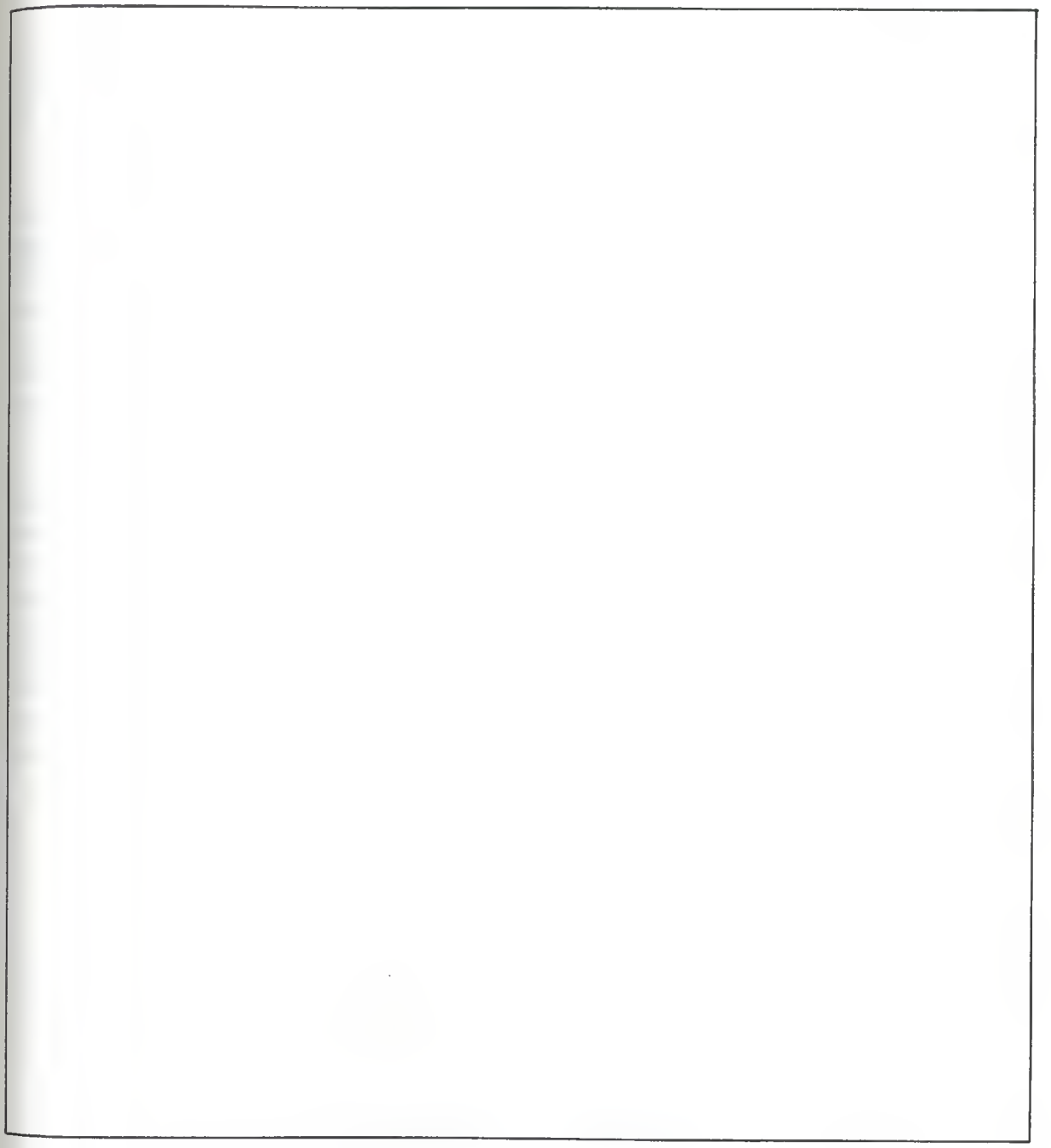
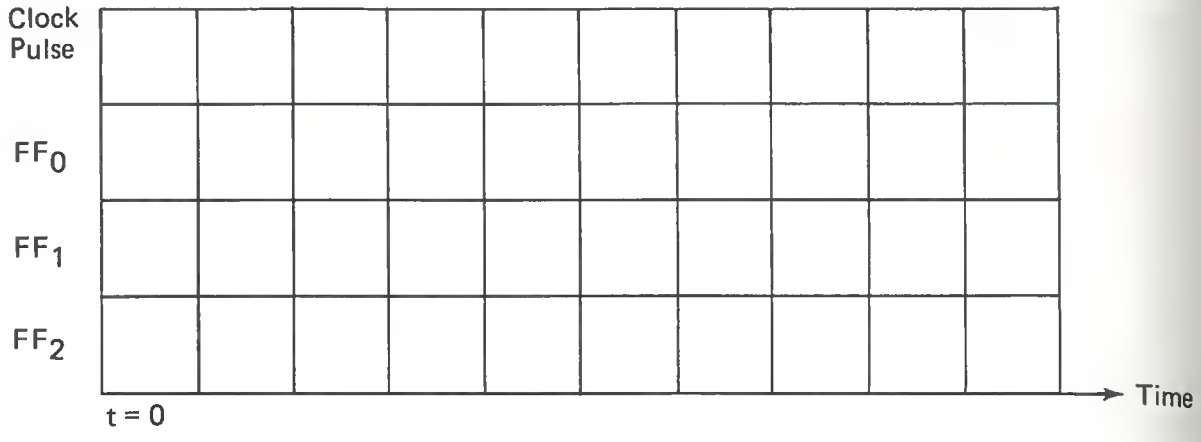


Fig. 19-8 The Data Tables

Pulse Train Data



Counting Data

Decimal Equivalent	CP	FF_2	FF_1	FF_0
0				
1	1			
2	1			
3	1			
4	1			
5	1			
6	1			
7	1			

Figure 19-8 The Data Tables (Cont'd)

PROBLEMS

1. How many FFs would be required for a 32-scale counter.
2. Describe the condition of the FFs for the binary count of 6.
3. What was the effect of the reset switch on the outputs of the binary counter?
4. What type of pulse triggers the FFs used (negative going or positive going)? Explain.

experiment 10100 RING COUNTER

INTRODUCTION. Counting is a very important operation in computers and in other logic applications. Many different types of circuits can be used to perform a given calculation within a computing system. In this experiment we will examine a ring counter. This circuit is one of the several ways in which electronic counting can be carried out.

DISCUSSION. A ring counter is a series of binary counters in which the output of the first is coupled to the second, the second to the third, etc. The output of the last binary is coupled back to the input of the first. In a ring counter, only one bistable at a time is allowed in the "1" state; all other bistables are in the "0" state.

This arrangement can be used as a decimal readout from a binary counter. The use of a "ring" makes decoding binary numbers to decimal easy. When the ring counter is used for readout, there must be one bistable multivibrator for each decimal number to be read. Each of the bistable inputs is omitted. When the counter is reset, the FF corresponding to decimal zero is turned on to the 1 state; all the others are switched to the zero state. A count pulse will supply the one to the next binary. At each count the one moves around the circuit until it reaches the last bistable and places it in the one state. The next count pulse sets the first bistable back to one. A count through the entire scale of the register is indicated when the first FF returns to one.

Before we discuss the actual ring counter to be used in this experiment, let us examine the integrated circuit that will be used to make this counter.

As you see in figure 20-1, the IC contains two J-K flip-flops which operate independently of each other. Each has two accessible outputs, Q and $\bar{Q}$, which are always in opposite states.

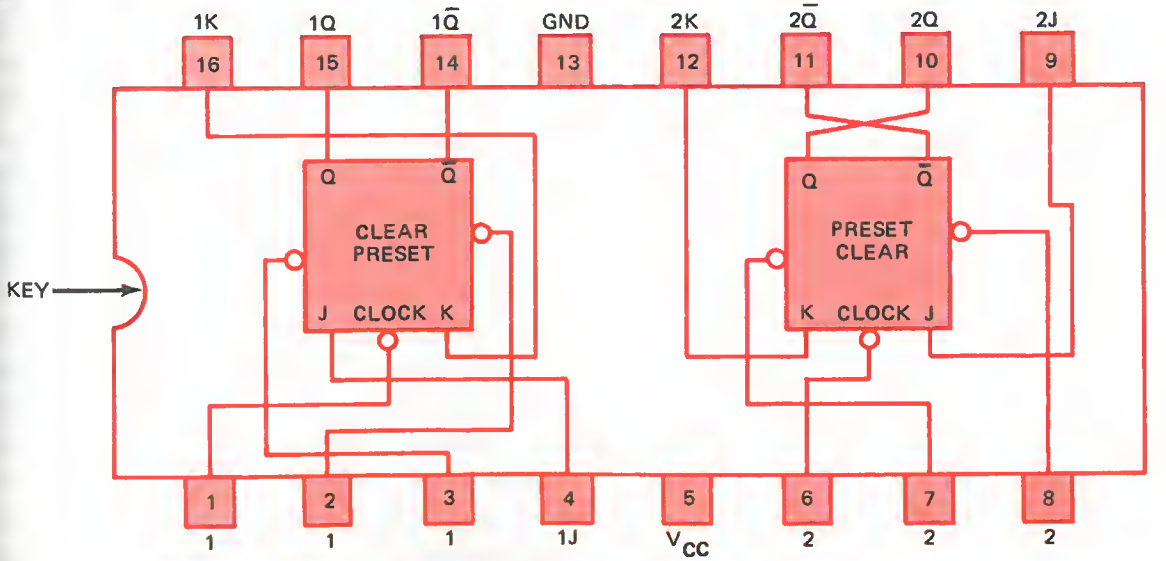


Fig. 20-1 The Integrated Circuit

Truth Table (Each flip-flop)		
t_n		$t_{(n+1)}$
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse positive logic

Fig. 20-1 The Integrated Circuit (Cont'd)

The clear and preset terminals operate independently of the clock, and may be applied either mechanically or electronically.

The transitions of the J-K flip-flops correspond to the truth table shown in figure 20-1. The desired input levels (not pulses) are applied to the J and K terminals and are kept constant while a negative going pulse is applied to the clock terminal. This pulse must be free of the bounce that is often characteristic of mechanical switches.

Figure 20-2 shows the block diagram of the ring counter to be used in this experiment. This counter contains six flip-flops, so it has a decimal readout capability of 5 if the first flip-flop is used to represent 0 or the reset state.

The important thing to note is that the count is applied to all of the FF devices at the same time. This count pulse has the same effect as a reset input to any device that is in the 1 state. The coupling between binary devices is to favor the proper binary so that it will respond, and the count will be passed to the next binary as desired.

The operation of the counter is as follows: The first move is to reset the system. This is done by momentarily closing the reset switch which applies a low input to the preset terminal of FF_0, putting it in the 1 state. At the same time the low input is applied to the clear terminal of FF_1 through FF_5 putting them in the 0 state. Now the system is ready to count.

The first count pulse is applied. The J and K inputs of FF_2, FF_3, FF_4 and FF_5 are all 0 before the pulse so these FFs will remain in the same state, which is logical 0. At the time of this first pulse, K_0 of FF_0 is 1, due to the feedback loop from Q_0. J_0 is 0, so FF_0 will make the transition from 1 to 0 and remain there. Before this pulse, the J_1 terminal of FF_1 is 1 due to its coupling to Q_0 of FF_0, and the K_1 terminal of FF_1 is 0 due to the feedback loop. Therefore, FF_1 will switch from the 0 state to the 1 state.

The next count pulse shifts FF_1 back to 0 and sets FF_2 to 1. In this manner, the count is passed around the ring until the sixth pulse, which returns the ring to its initial (preset) condition. The system can be returned to the reset state at any time by use of the reset switch.

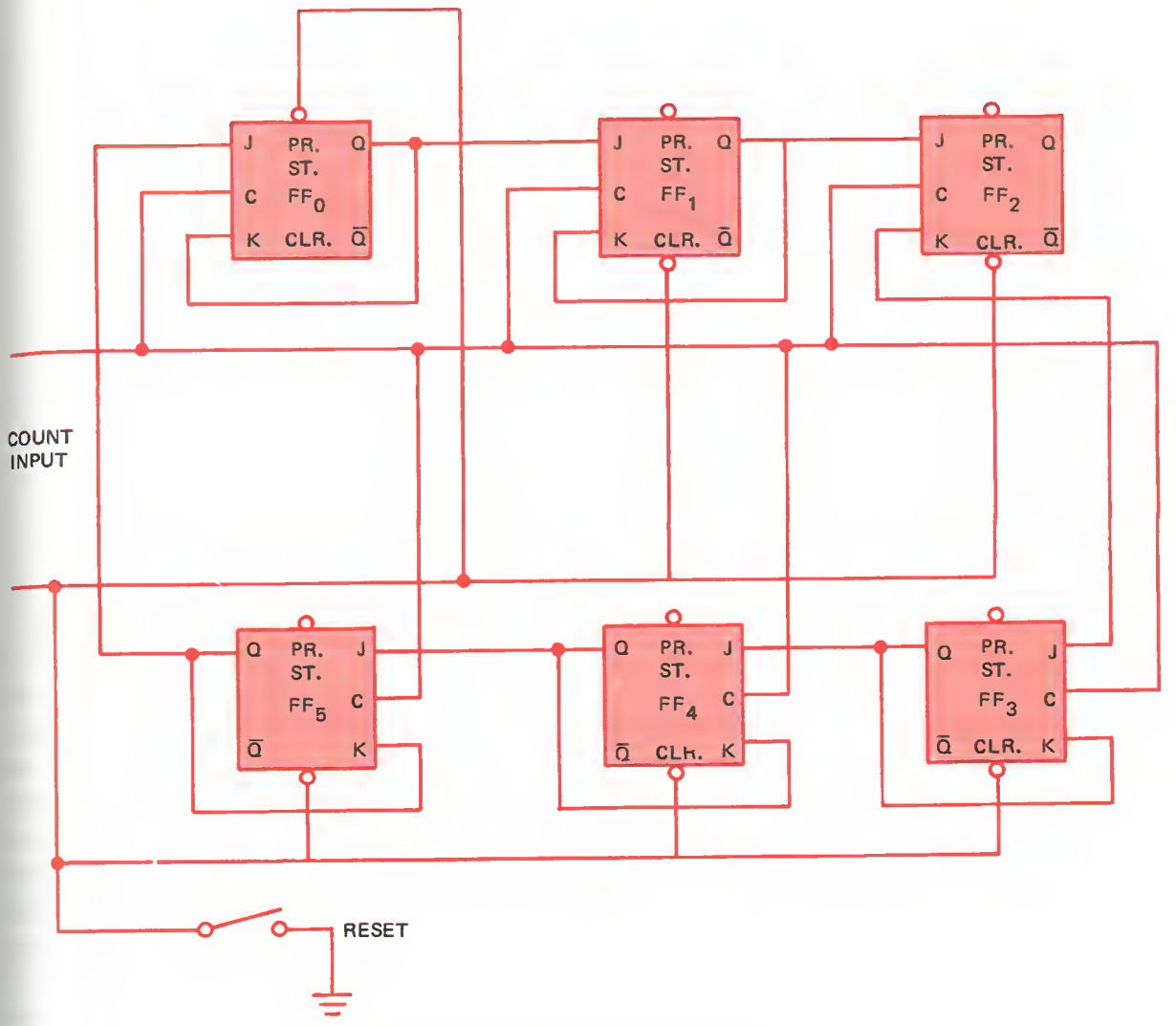


Fig. 20-2 The Ring Counter

Each flip-flop has a transition time T_t of about 50 ns. This is the time it takes the flip-flop to respond to a clock pulse. If there are N stages (or binary devices) in a counter like the one shown in figure 20-2, the minimum time possible for the counter to make one complete ring is N X T_t. Therefore, the output of any stage is a pulse train with a minimum period NT_t, and the duration of each pulse is the time T_t.

Ring counters are used in applications where sequential gating is required. The system may be thought of as a stepping switch in which each count advances the switch one step. The outputs can be fed to succeeding circuits at each point with regard to the *fan-out* limitation of the ICs being used. (This fan-out limitation is given in the data sheets for the devices.)

Any type binary device may be used as a counter. Typical of these binary devices are transistor flip-flops, unijunction transistors, tunnel-diodes, and silicon-controlled rectifiers.

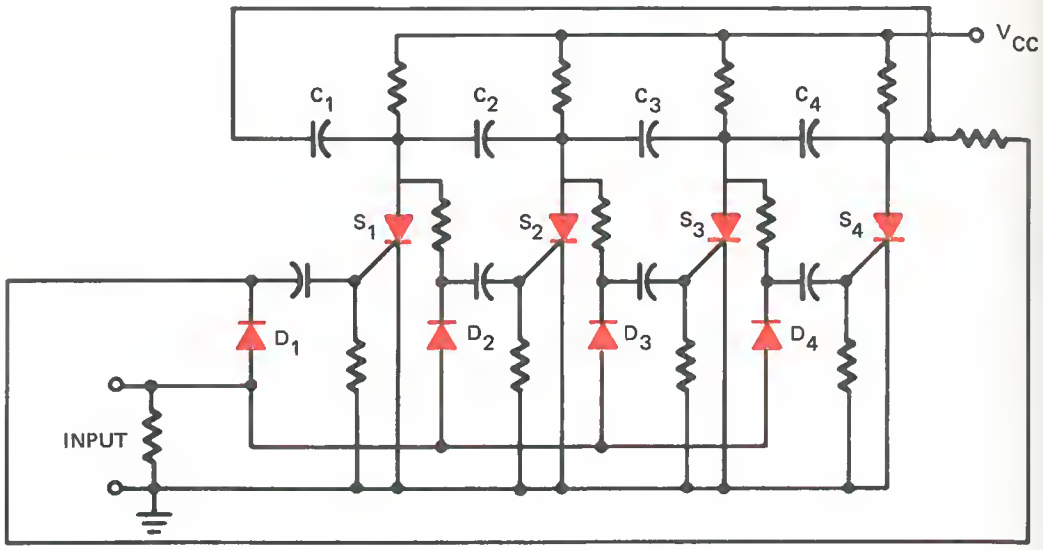


Fig. 20-3 SCR Ring Counter

For instance, consider the SCR ring counter in figure 20-3. In this circuit, the counting pulse is positive. Each of the anodes is coupled through a capacitor to the anode of the next SCR. S_1 is triggered to start the ring, and all of the other devices are off. All of the diodes are reverse biased by V_{CC} except D_2, which is only slightly reversed biased because S_1 is on. This diode D_2 will accept a trigger pulse which is only slightly smaller than V_{CC} in amplitude and positive. This pulse will be transmitted through D_2 to the gate of S_2 and S_2 will switch on (logical one). When S_2 switches on, an abrupt drop in voltage occurs at its anode. This voltage change will be transmitted through C_2 to the anode of S_1, which drops below its maintenance voltage and turns off. Thus, the action is much the same as was described for the J-K FF counter. The first binary device starts out in the on condition, a count pulse turns on the next one and resets the first. The diodes or gates select the device that is in proper condition for change. This same principle applies to fluid switching devices and works well with fluidic flip-flops.

MATERIALS

1 DC power supply (0–40V)
3 Integrated dual J-K flip-flops, type SN7476N or equivalent
1 Integrated dual J-K flip-flop, type SN15845N or equivalent
4 In-line IC sockets (SN7476Ns have 16 pins; SN15845N has 14 pins)
1 Set of data sheets for each IC type
1 Oscilloscope
1 Function generator
1 SPST switch
1 DPDT (center-off) switch

PROCEDURE

1. Examine your ICs. Construct a "triggering circuit" using a DPDT switch from the set or reset terminal of the SN15845N (or equivalent) to ground. V_{CC} should be 5 volts.

2. Connect the output of your "triggering circuit" to the clock terminal of one of the other ICs. Use V_{CC} = 5V. Experimentally determine the truth table for the ICFF. Record your results in the data table.
3. Now construct the 5 scale ring counter shown in figure 20-2. Use the "triggering circuit" to apply count pulses. Measure V_{CC} to be very sure it is not over 5 volts.
4. Record the states of all the FFs (values of Q) when the reset switch is tripped. Use 1s and 0s, not actual voltage levels.
5. Record the states of all the FFs after 1, 2, 3, 4, 5, and 6 count pulses are applied.
6. Record the response of the counter if the reset switch is tripped after a count less than 5.
7. Disconnect the supply voltage and the "triggering circuit" from the counter.
8. Connect the function generator (pulse output) to the counter so that +4.5 volt pulses will be applied to the count circuit.
9. Adjust the generator so that approximately 20 pulses may be viewed on the scope.
10. Sketch the input waveform and the waveform of at least 2 FFs. Also sketch the waveform of $\bar{Q}$ of 1 FF.
11. Observe the waveform of the counter if the reset switch is held closed while a pulse train is being applied.

ANALYSIS GUIDE. In analyzing these results you should discuss the characteristics of the ring counter and the use of the IC modules for its construction. A complete discussion of the "Pulse Train Data" should also be included.

Truth Table		
t_n		$t_n + 1$
J	K	Q

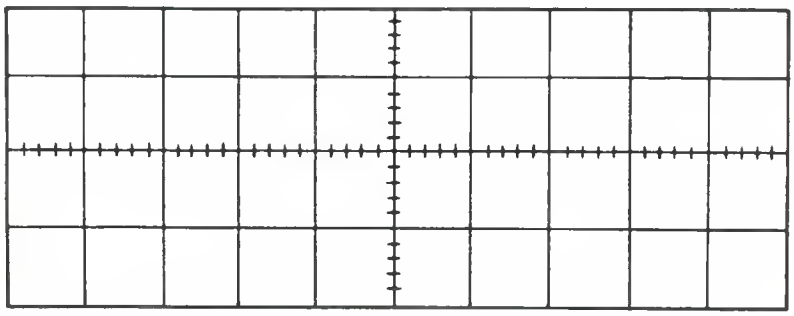
Fig. 20-4 The Data Tables

Ring Counter States							
Input	Reset	1	2	3	4	5	6
FF_0							
FF_1							
FF_2							
FF_3							
FF_4							
FF_5							

Effect of reset when count $<$ 5 was _____

_____

_____



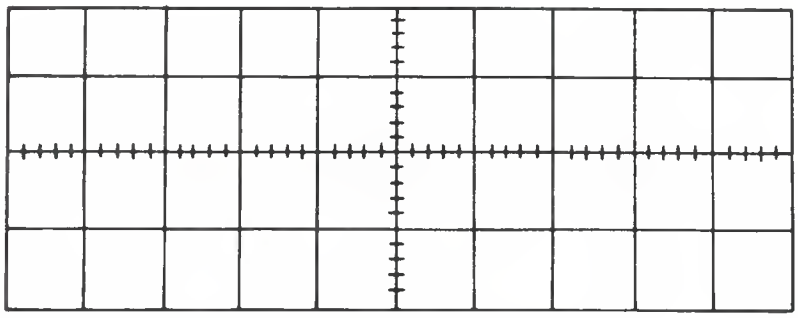


Fig. 20-4 The Data Tables (Cont'd)

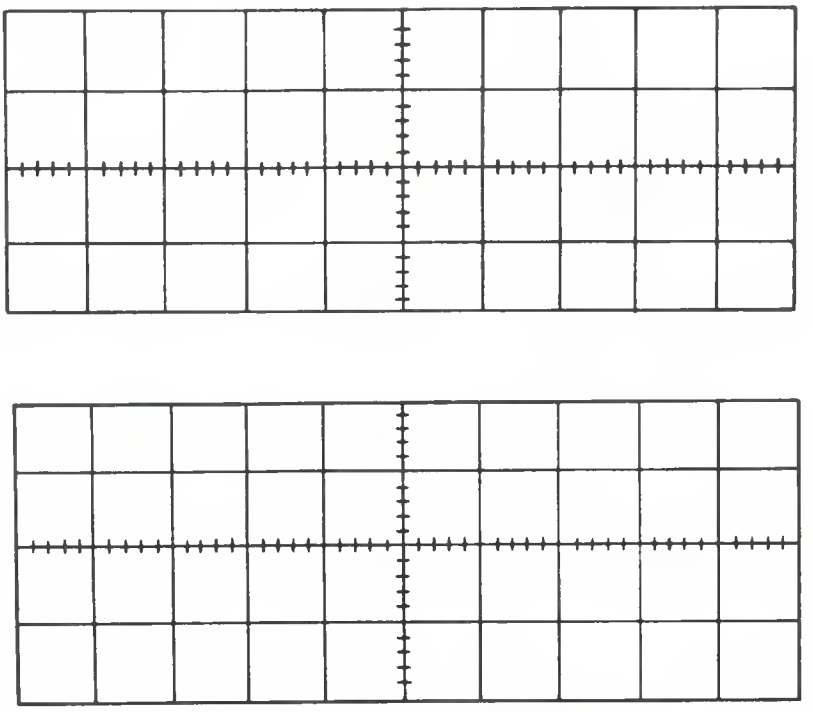


Fig. 20-4 The Data Tables (Cont'd)

PROBLEMS

1. What is the scale of count for the circuit in figure 20-2?
2. From the data sheet, what is the maximum fan out capability of the ICs you used?
3. What is the power dissipation of your ICs?
4. What is the maximum frequency of a pulse train that can be applied to the counter used in the experiment?

experiment 10101 SHIFT REGISTERS

INTRODUCTION. The arithmetic operations of a computer depends on the storage and processing of binary numbers. One of the circuits is a register. A particular kind of register which can shift the binary number to either the right or left of the binary point is called a shift register. In this experiment we will examine the operation of a simple shift register.

DISCUSSION. Data storage in a shift register is usually very temporary, sometimes for only a few microseconds. Because of this short storage time, bistable devices are used extensively. Therefore, most shift registers are made up of binary devices coupled together.

Flip-flop circuits are normally connected in series, with the output of the first connected to the input of the next and so on. Clock pulses (the pulses to be counted) are fed to the input binary and stored. The first pulse to be stored sets the first flip-flop. The second pulse resets the first FF and causes the transfer of the first stored pulse to the next FF circuit. Thus, as each pulse appears at the input, a shift of pulses occurs down the string of flip-flops. The new pulses are pieces of information (called *bits*). So you see, every time a pulse appears, information is shifted from one binary to the next and a new "bit" is entered into the first. Many bits can be stored in this way (depending on the number of flip-flops) until the information is called for on command or after some predetermined length of time.

The term shift register arises because the particular circuit of interest here is used to shift the number either to the right or to the left of the binary point. Shifting to the left is, in effect, multiplication by two. Shifting to the right is, in effect, division by two. The 0 and 1 outputs of one state are taken to the R and S inputs of the next stage. The bits are transmitted unchanged from stage to stage.

Let's look at the symbol for a flip-flop in figure 21-1. In the usual case, the 1 and 0 output lines are each the collector of a transistor. The 1 side is chosen arbitrarily. After choosing the 1 side, the set (S) input is the input that causes the 1 side to go to the one condition. The reset input then, will switch the side to the one state. The T or trigger input is the complementing input.

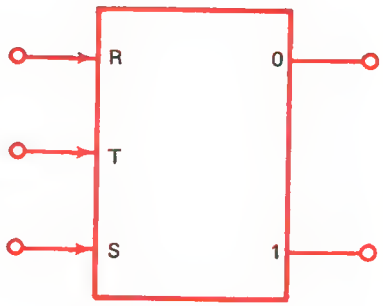


Fig. 21-1 Flip-Flop Symbol

Complementing is, in effect, simply the inverting of the flip-flop. The state of the FF will be changed by proper input pulses at T. If the binary is in the S state, output 1 = 1 and a pulse is applied at T; then the binary will switch to the opposite state. To complement or invert the state, a zero potential can be applied to the collector of the nonconducting transistor, or to the base of the conducting transistor (all else remaining constant and compatible). In most cases of counting and shifting, a special input trigger network or gate would be used.

Let's interrupt our discussion of shift registers to discuss one basic circuit which

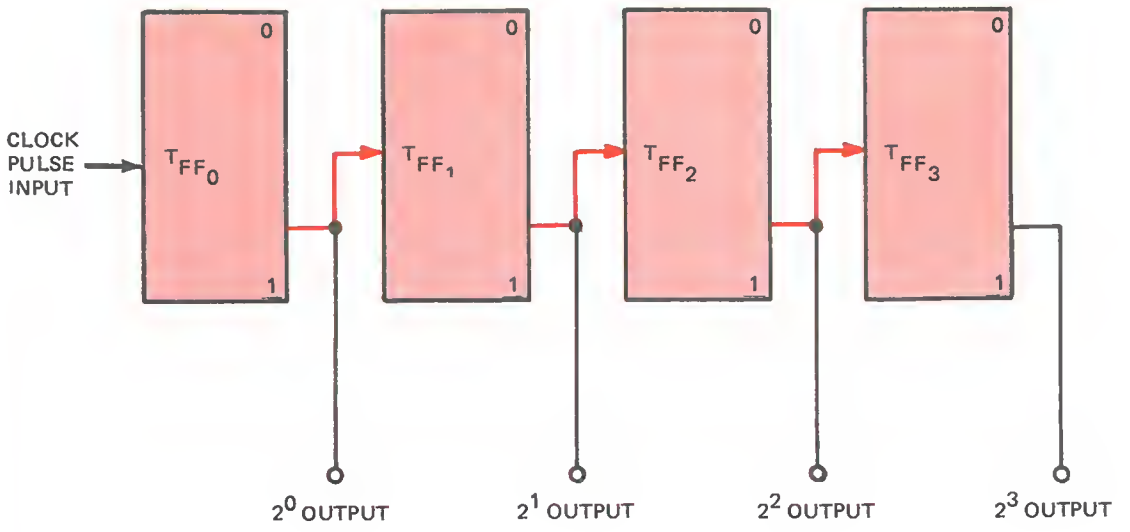


Fig. 21-2 Four-Stage Binary Counter Using J-K Mode

often serves as an input trigger network. Figure 21-2 shows a simple binary counter. As you can see in this circuit, the interconnection of these FFs is such that the 1 output feeds the trigger input of each successive unit. With each negative-going input clock pulse, the FF_0 (2^0) state is complemented. NPN circuits will be so complemented only when the input voltage pulse is sloping negatively. For positive logic (which is rarely used in practical applications) the FF would trigger on positive pulses. Positive logic is defined as + volts = logical 1, 0 volts = logical 0.

Getting back to the NPN logic, with the first input trigger causing an output at the 2^1 stage to go from 0 to 1, the FF_1 stage (2^1) will not complement (switch) because the slope is of the wrong polarity. The second pulse complements (switches) the FF_0 (2^0) stage from 1 to 0. This time the switching is in the proper direction to cause the FF_1 stage to complement. However, the polarity is wrong to complement the FF_2 stage, etc. Figure 21-3 shows how these operations are carried out one pulse at a time. The binary count is equal to the input pulse number, and increases as the count progresses. That is, pulse one corresponds to FF state 0001 (binary 1), pulse 2 corresponds to 0010 (binary 2) in the up or increasing direction. This type counter is referred to as an **up** counter. There are 2^n counts with an n stage counter. It is interesting to note here that the circuit of figure 21-2 can be thought of as a frequency divider, with the frequency of each stage being the input frequency divided by 2^{n+1} where n = the number of the output stage.

$$\text{Frequency} = \frac{\text{input frequency}}{2^{n+1}} \qquad (21.1)$$

These types of counters are referred to as binary accumulators or adders. If n pulses are fed to the input, the register goes to binary n. Then if n′ additional numbers are fed to the input, the register goes to the n + n′ binary number. In specific terms, three pulses will store as binary 3 (11). Two more pulses at the input cause the count to go to binary 5 (101). Up counters are used in this way for addition.

Input Pulse No.	FF_3 Output 2^3	FF_2 Output 2^2	FF_1 Output 2^1	FF_0 Output 2^0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16/0	0	0	0	0

Fig. 21-3 Four-Stage Up Count

In order to divide, the reverse counting operation must take place. Figure 21-4 shows a circuit for counting down. Each successive stage operates at a slower rate. Notice that the difference is that the zero side now feeds the trigger input. Also note that the frequency dividing characteristics remain the same (because the outputs are taken from the same point). It is easily seen that the only difference between up count and down count is the side of the FF used to trigger the input. Arithmetic operations require that the 1 side be used for addition and the zero side for subtraction. Actually this simplified arrangement is seldom used but the principle is valid. Figure 21-5 shows the table of count down operations for four stages. In this case the pulse count corresponds to the complement of the decimal output.

A method more frequently used consists of a combination of these two simplified

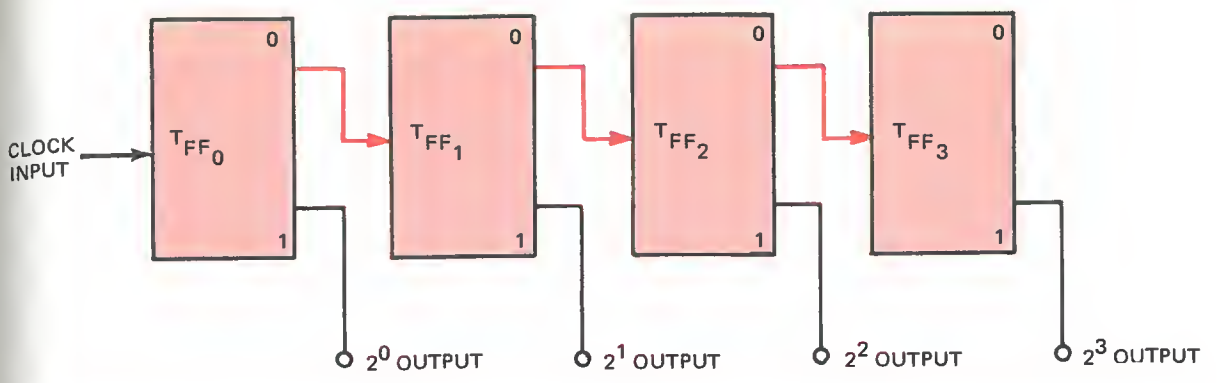


Fig. 21-4 Four Stage Down Count Register (All FFs in J-K Mode)

Input Pulse No.	FF_3 2^3 Output	FF_2 2^2 Output	FF_1 2^1 Output	FF_0 2^0 Output	Decimal Output Count
0	0	0	0	0	16 or 0
1	1	1	1	1	15
2	1	1	1	0	14
3	1	1	0	1	13
4	1	1	0	0	12
5	1	0	1	1	11
6	1	0	1	0	10
7	1	0	0	1	9
8	1	0	0	0	8
9	0	1	1	1	7
10	0	1	1	0	6
11	0	1	0	1	5
12	0	1	0	0	4
13	0	0	1	1	3
14	0	0	1	0	2
15	0	0	0	1	1
16/0	0	0	0	0	0/16

Fig. 21-5

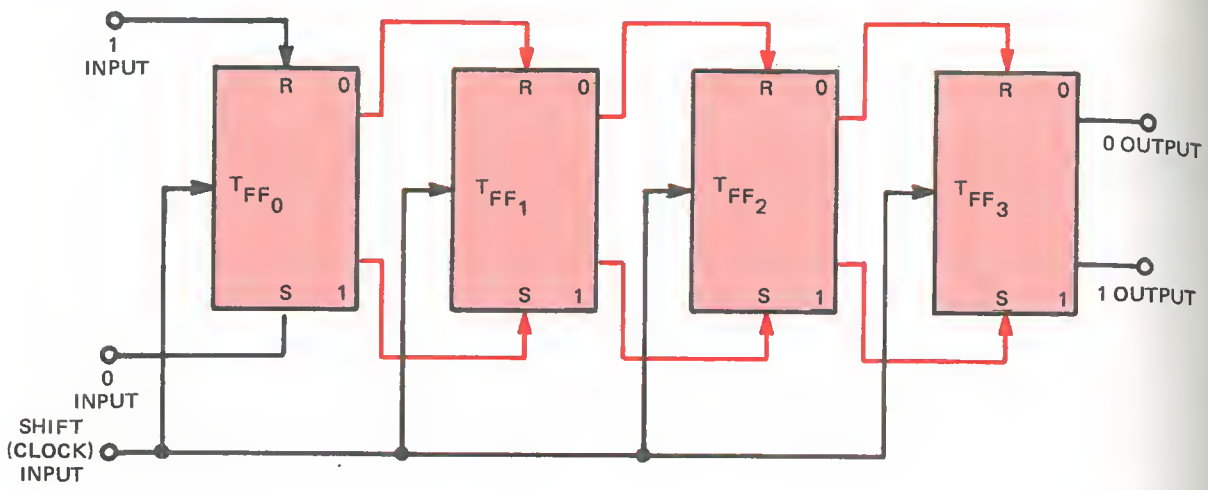


Fig. 21-6 Four-Stage Shift-Right Register

methods with suitable coupling to allow shifting from one mode to the other. By using steering gates, the input FF can be controlled by the condition of the remaining binaries, and the result is a circuit which can allow shifting of stored information (bits) from one stage to the other. Variations can be made in the gating to shift bits to the stage on its right, or to the stage on its left.

Figure 21-6 shows the circuit for a shift-right register using R, S and T flip-flops. As data is fed into one side of the register, it is shifted serially, one bit at a time (corresponding to one shift per pulse). Each shift moves all pulses over one bit. Figure 21-6 will move the pulses one bit at a time to the right. Shifting to the left can be accomplished by using a circuit similar to figure 21-7. This circuit is the complement of the figure 21-6 circuit and the inputs and outputs are exchanged.

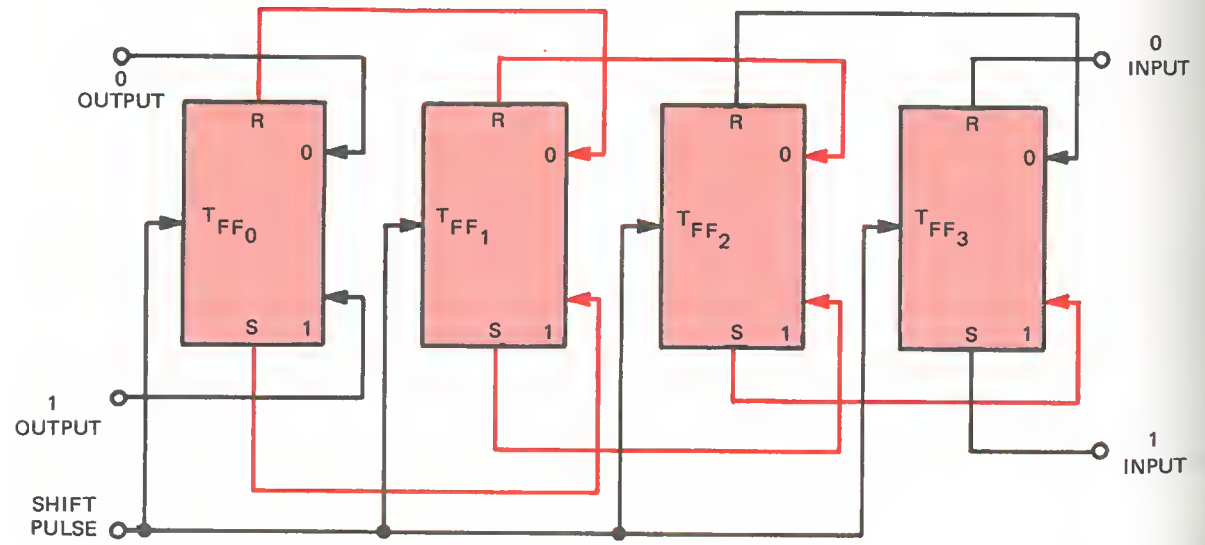


Fig. 21-7 Four-Stage Shift-Left Register

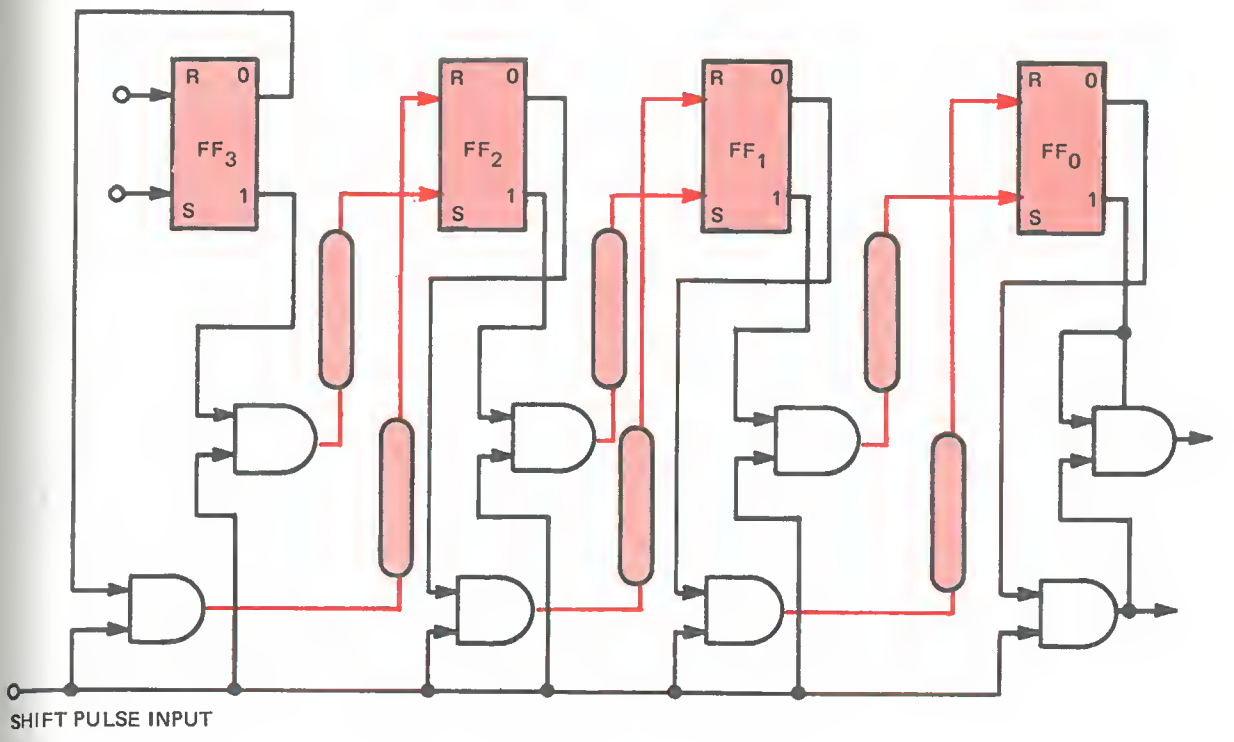


Fig. 21-8 Broadside Shift Register

Actual computing circuits require somewhat more gating than is shown in either figure 21-6 or 21-7. Figure 21-8 shows a broadside shift register in which all bits are shifted from one to the next simultaneously. You will notice that this is a right shift circuit and would be used for division. Delay lines are shown between the output of the gates and the S and R inputs. These are necessary for practical circuits to insure reliability. The delay lines make certain that the content of one binary is transferred before new information is stored. As always, set and reset as well as 0 and 1 inputs are defined arbitrarily but they must remain consistent.

In operation, when a shift pulse is applied, only those AND gates with 1 inputs from the FFs will respond. These gates will then apply pulses to the set or reset inputs of the next binary and shift the count. This circuit provides a division shift and its complement would provide a multiplication broadside shift.

One other type shift register is used extensively and gets around the need for the delay lines to avoid the "race" problem. The ripple shift register allows the count to ripple through the circuit, changing one FF at a time. Figure 21-9 shows a ripple shift to the left.

The shift pulse is applied only to the first two gates. One of these gates will operate with FF_1 in a particular state. Whichever gate operates it will set or reset FF_2. Through the first OR gate and the second pair of AND gates (3 and 4), the selection of state of FF_3 is made and FF_4 is set or reset accordingly. Again we have explained the circuit in terms of positive logic because it is easier for the beginner to understand. The actual circuits normally use negative logic NAND and NOR gates with negatively pulsed FFs.

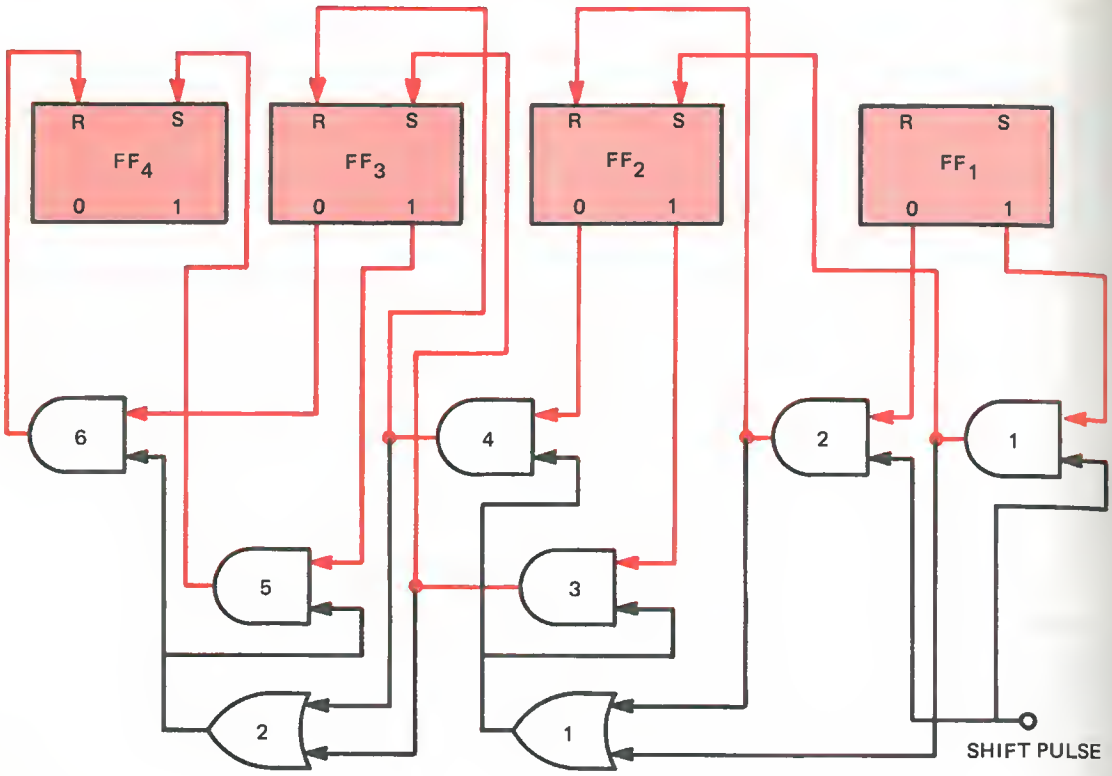


Fig. 21-9 Ripple Shift to the Left

As we have said the most common type of register is the serial or shift register. The term implies a number of FFs in series, the output of one feeding the input of the next. Clock pulses are fed to all the FFs. When the clock pulse appears, a bit at the set input is moved to the first FF where it is stored. The next clock pulse causes the bit to transfer to the next FF, etc. Several bits may be stored one bit per stage. They can be stored for any length of time and retrieved on command.

The foregoing discussion has been general but would lead the reader to think of discrete logic or logic blocks. In reality, the present generation of computer uses integrated circuit logic almost exclusively. Whole registers are often contained on a single chip. The trend, in fact, is toward large scale integration (LSI), which includes many of the functions of the present day operational computer on a single chip. Also very common for economical and practical reasons are medium scale integrated circuit modules (MSI).

One such module is a consumer-type 8-bit shift register. Its logic and package diagram is shown in figure 21-10. This unit is a typical standard integrated circuit shift register. Set reset (SR) flip-flops are used with an input gate and an inverter for complementary pulses at the S and R inputs of FF_0. The clock pulses are inverted also. Figure 21-11 shows the input output clock relationship. Notice that the output pulse appears eight clock pulses later, and is the width of two clock pulses in that the binary does not shift until the start of the next clock pulse. Negative pulses are required to trip the NOR gate. The clock pulses are required to be at least 25 ns wide and can be as fast as 18 MHz.

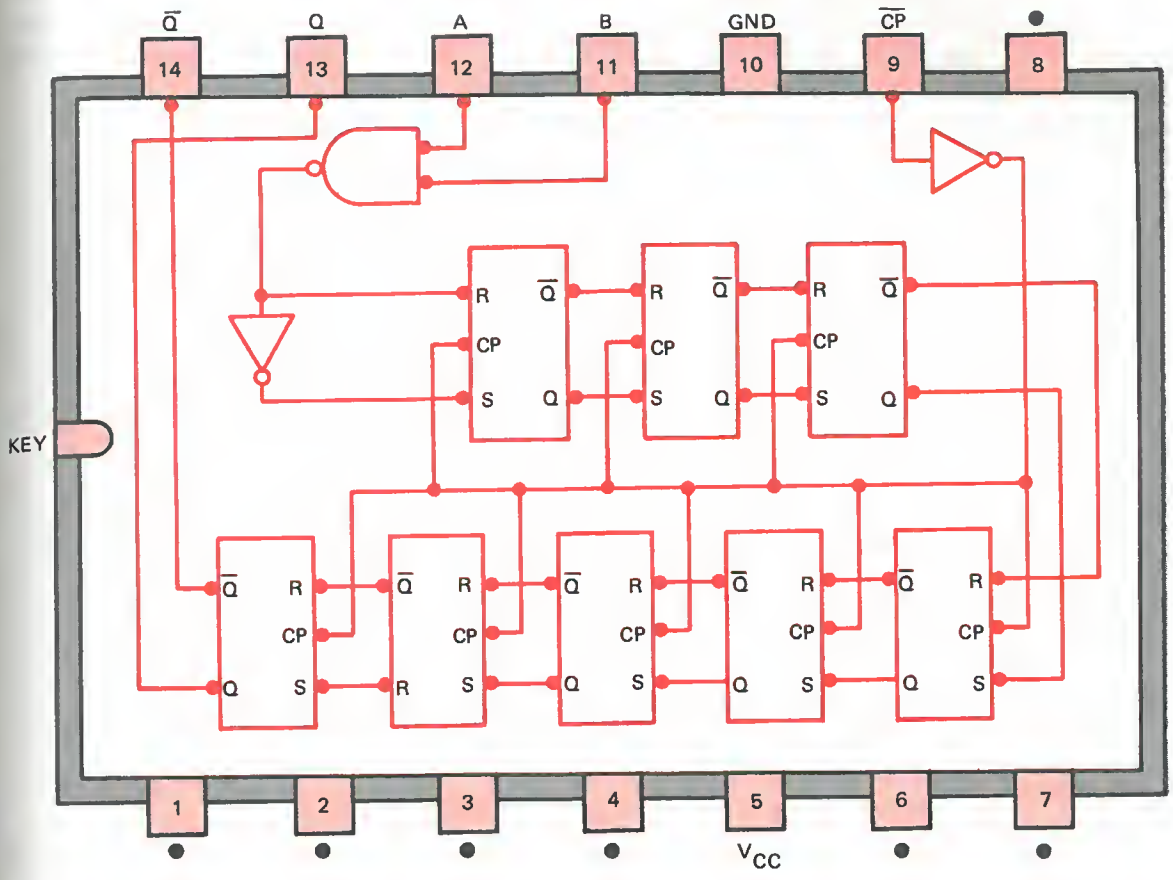


Fig. 21-10 Logic and Package Diagram of an 8-Bit Shift Register

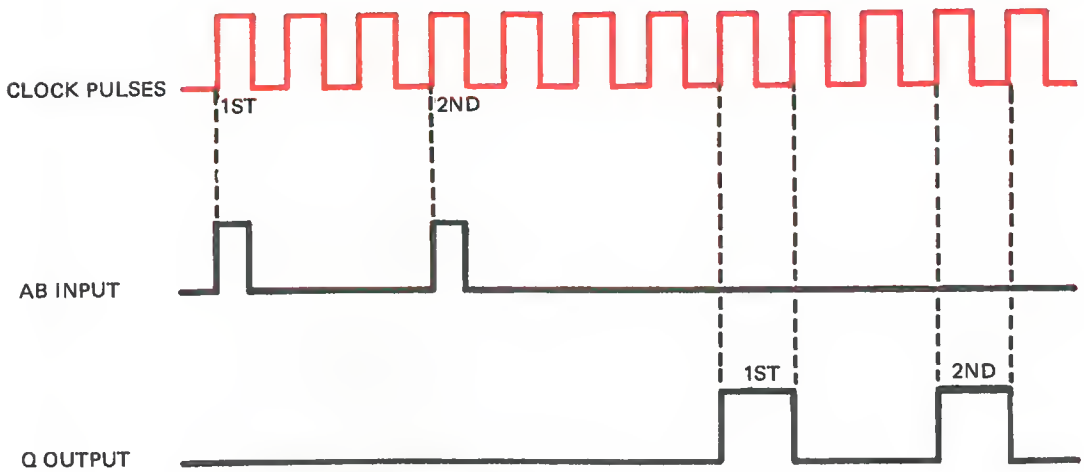


Fig. 21-11 Input and Output Waveforms for 8-Bit Shift Register

The unit uses transistor-transistor-logic (TTL), which is similar to diode-transistor logic but the diodes are replaced by multi-emitter transistors. This unit actually includes 4 gates for each binary giving a total of 35 gates. The silicon chip itself is 55 X 110 mils and the total power dissipation is about 175 mW. The unit will drive 10 other gates.

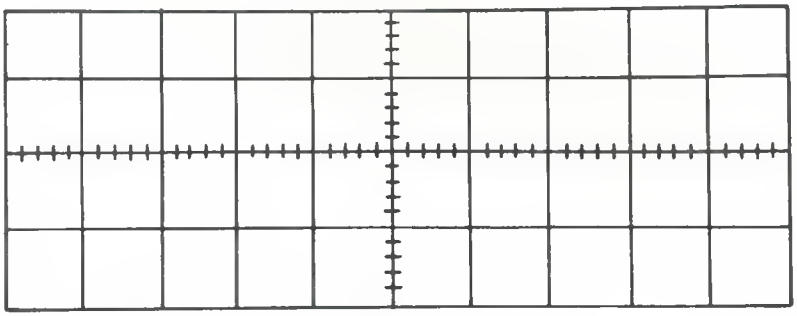
MATERIALS

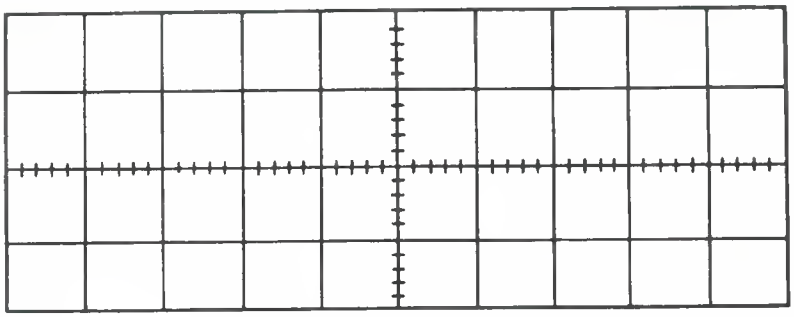
1 Oscilloscope
1 DC power supply (0 - 40V)
1 8-bit shift register, type SN7491AN
or equivalent
5 J-K/RS flip-flop, type SN15845N
or equivalent
6 IC sockets
1 Data sheet or equivalent for
each type of IC
1 DPDT center-off switch
1 VOM or FEM
1 Function generator

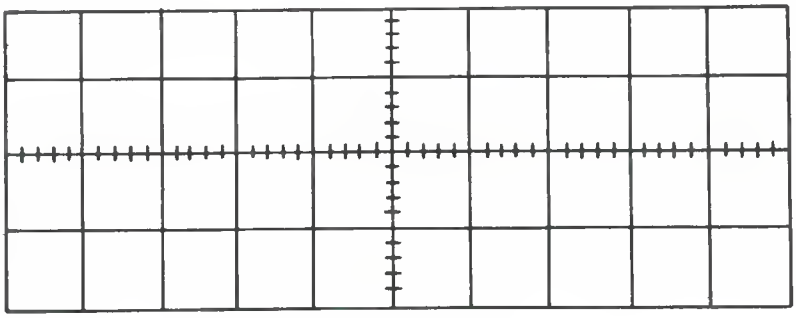
PROCEDURE

1. Examine the data sheet for the ICs involved. Note V_{CC}, rep rates, pulse width, and fan out.
2. Arrange the JK/RS flip-flops in a four-bit shift register. Include a "triggering circuit" constructed by shorting either the set or reset terminal of one FF to ground through the DPDT switch. Use $V_{CC} = 5V$.
3. **Before applying power, place an accurate meter across the power supply and make sure that V_{CC} does not vary more than 0.5 volt.**
4. Have the lab instructor check your circuit.
5. Apply power to the circuit.
6. Note the operation of the register, especially how many clock pulses were necessary to shift a given input completely through the register. Draw a sketch of the output trains for given input and clock pulse trains.
7. Study the data sheet of the 8-bit shift register. Then repeat steps 3 through 6. It is still necessary to use the "triggering circuit" to supply the clock pulses.

ANALYSIS GUIDE. The analysis of these data should contain observations on the characteristics of the shift register and IC application of the logic theory. Discuss each of the circuits used. Was their operation identical? Which was easier to work with? Why?







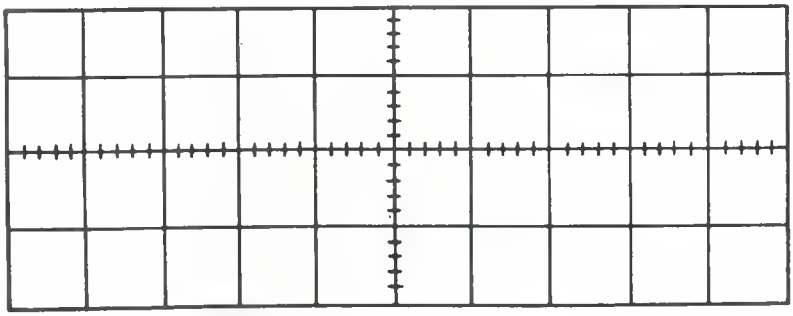
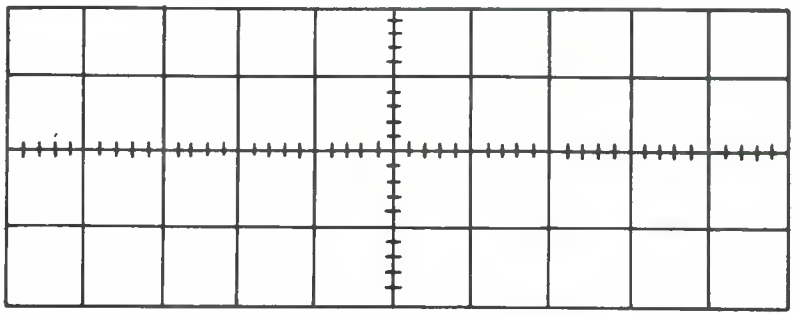
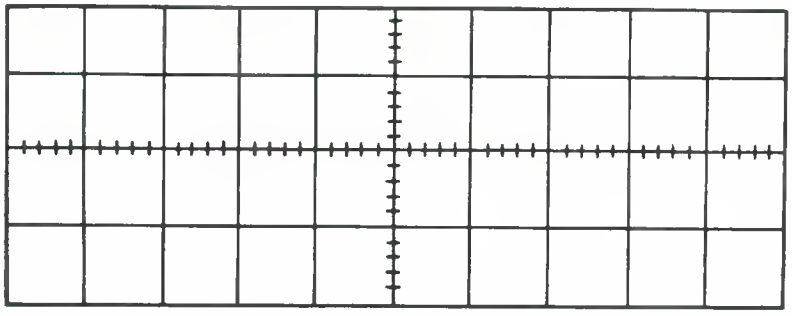
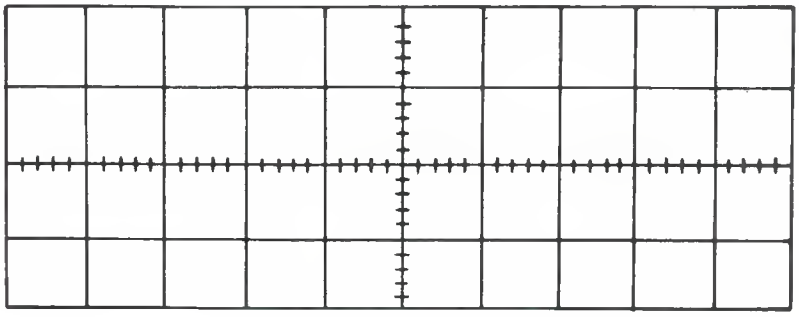


Fig. 21-12 The Results







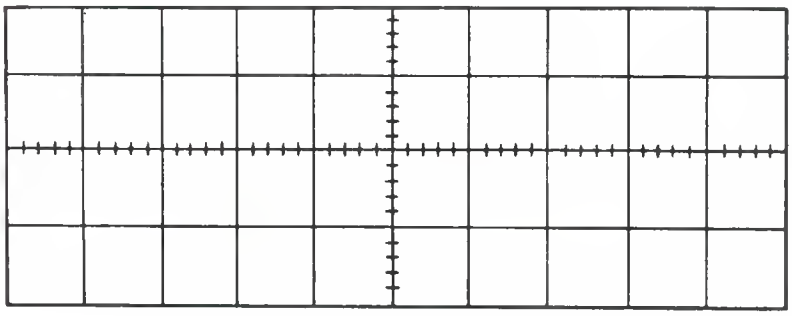


Fig. 21-12 The Results (Cont'd)

PROBLEMS

1. A PNP flip-flop triggers on a positive-going voltage change. What triggers a NPN flip-flop?
2. A frequency of 256 kHz is fed to the input of an up counter. What is the frequency of the 2^3 output stage? Show a block diagram and explain fully.

experiment 10110 DIODE MATRIX CIRCUITS

INTRODUCTION. Digital logic systems require that numbers and instructions be translated into the form of level shifts or pulse trains. Interpretation of these levels or trains requires some kind of translational network. One such network is a diode matrix. The basic purpose of a diode matrix is to encode or decode the digital information. In this experiment we will examine how this is done.

DISCUSSION. Encoding and decoding in digital computers can be done with logic gates even though the number of gates required is relatively large. The gate method has usually been used in small step decoding and encoding within digital computers. As an example of the problem, a two-stage counter for four steps requires four gates. Consider a 64-step, six-stage counter. Sixty four gates with six inputs each would be necessary; a minimum of 384 diodes would be required with this method. A diode matrix can reduce this number considerably.

At first, the statement above does not seem to be entirely true. Figure 22-1 shows a diode matrix for decoding three variables. Both are true (2^0) and false (2^{-0}) inputs

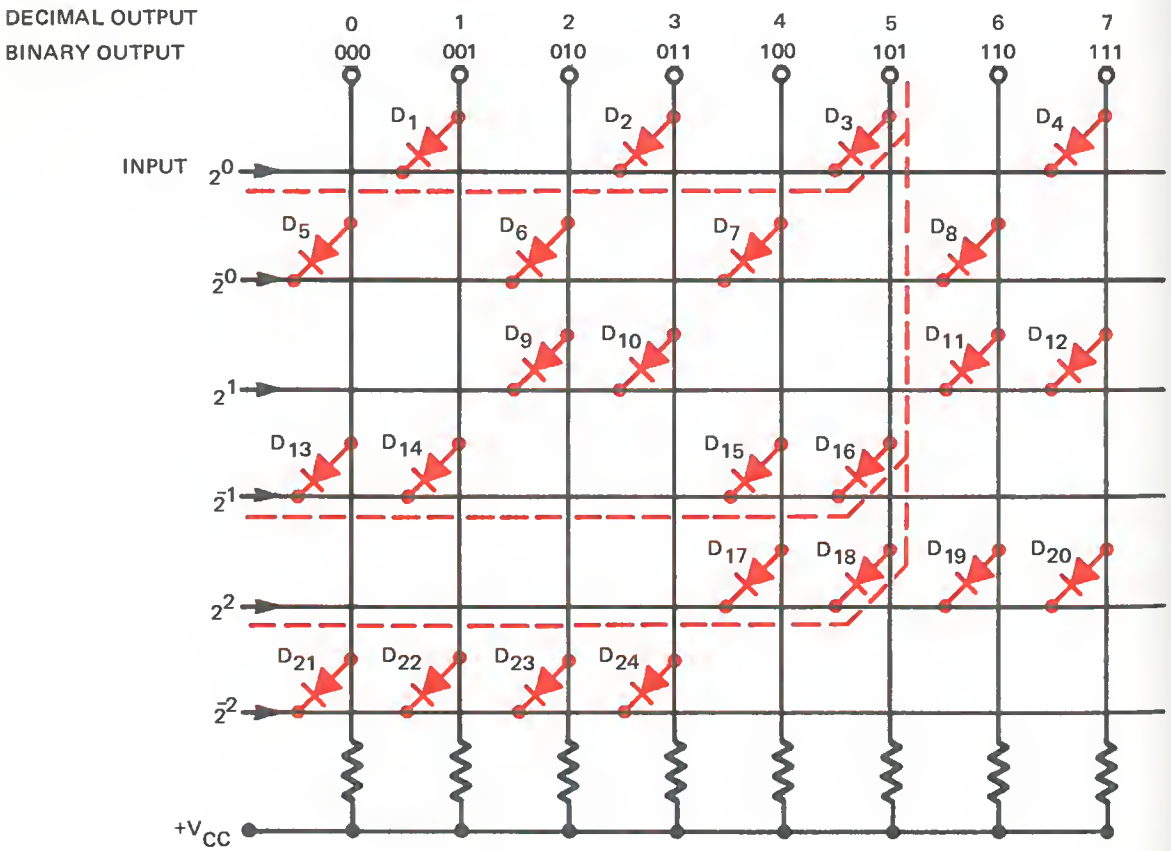


Fig. 22-1 Diode Matrix For Decoding Three Variables

are available. Half of these will be 1 and the other half will be 0 at any given time, but for each input combination, a different output line is high (logical 1). For example, diodes D_1, D_2, D_3, D_{13}, D_{14}, D_{15}, D_{16}, D_{17}, and D_{18} are back biased by positive voltages with inputs for a decimal 5 or binary 101. These lines are high or logical 1. The low (logical 0) signals present at the other inputs clamp all these lines to zero and, therefore, only the 101 (decimal 5) line will produce a high output. The most serious problem with this scheme is that it requires

$2^N \times N$ = Number of Diodes Required **(22.1)**

A six-stage matrix counter still requires 384 diodes which represents no improvement over separate gates.

A trick has been developed to decrease the number of diodes by making some of them perform double duty. This method is called *treeing,* and it decreases the number of diodes required dramatically. The schematic representation of a diode tree is shown in figure 22-2.

Looking back at the standard diode matrix in figure 22-1, we can see that the four diodes connected to the 2^2 and the 2^{-2} lines

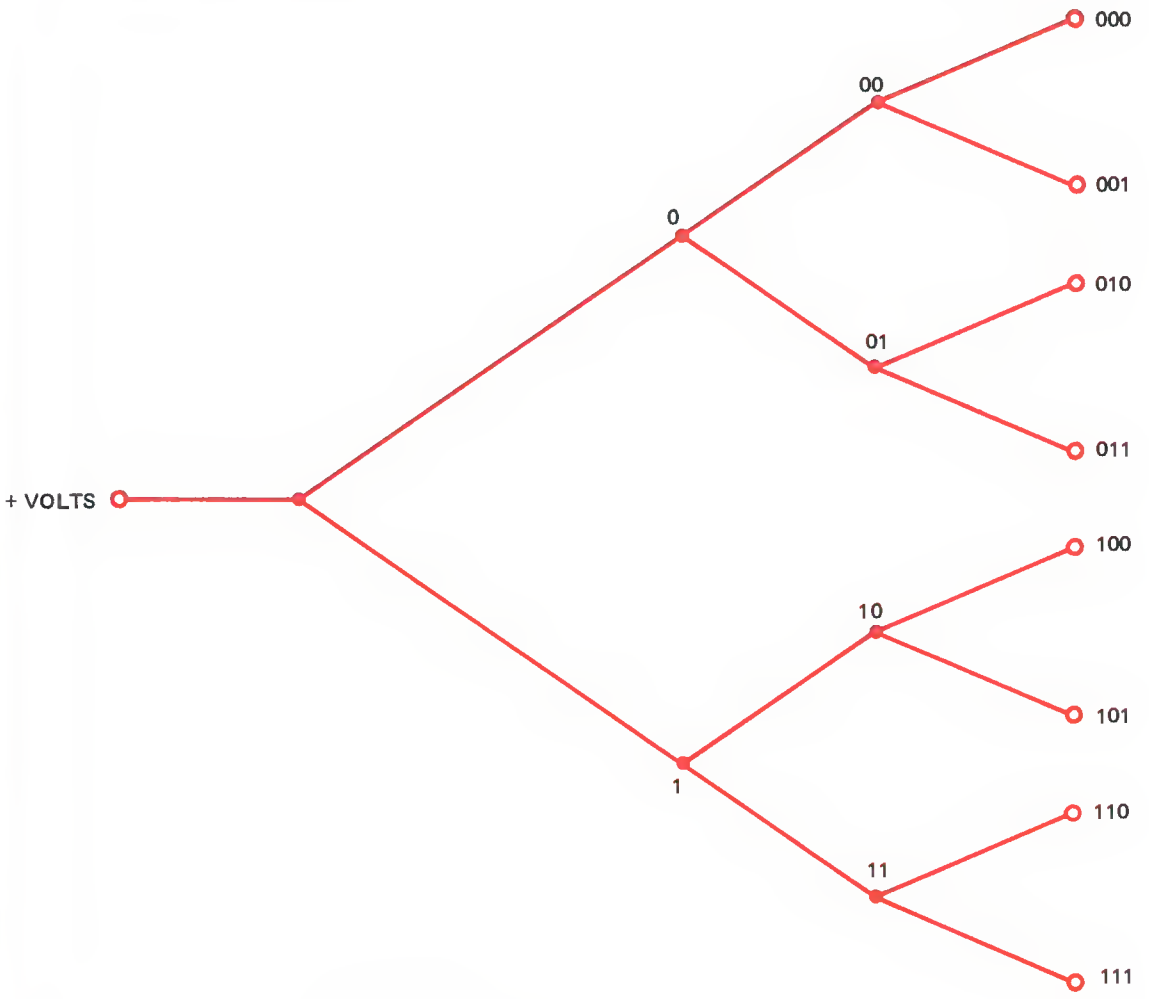


Fig. 22-2 Diode Tree Connections

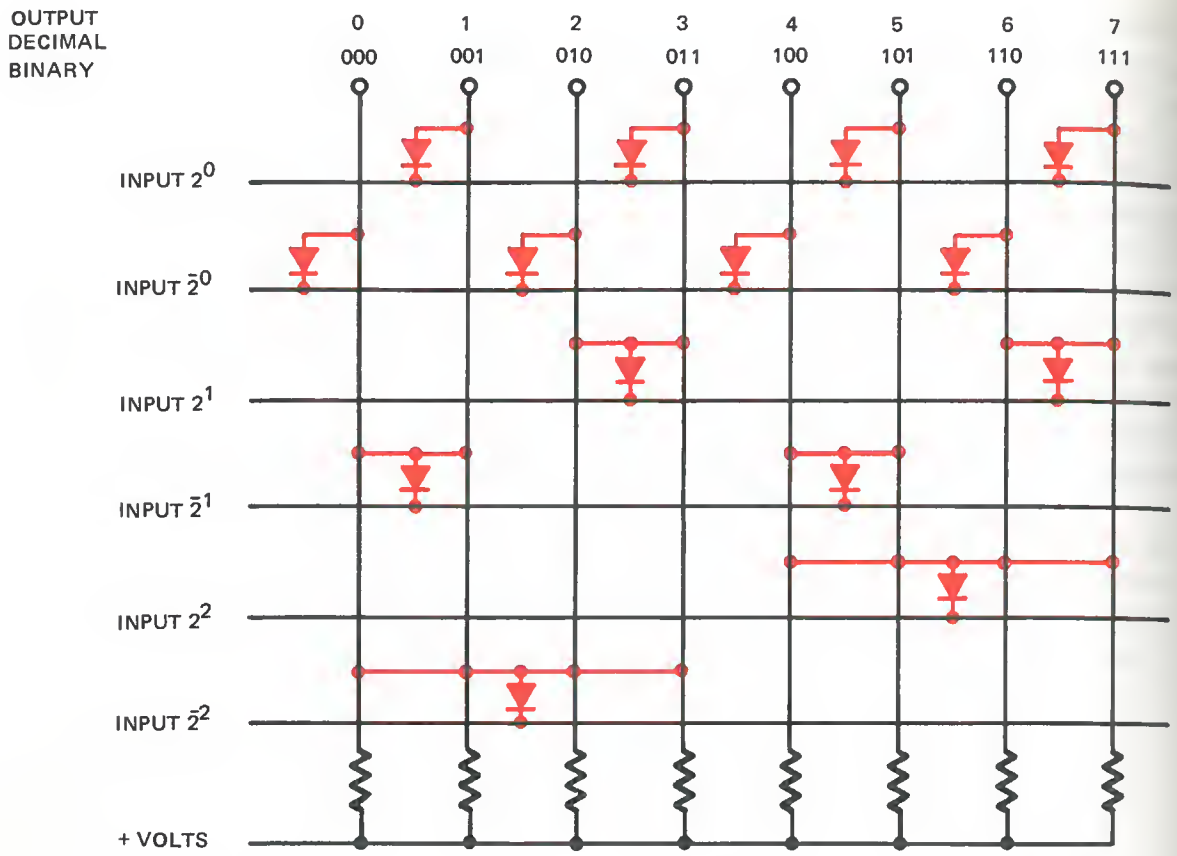


Fig. 22-3 Actual Connection of Diode Tree Matrix

could be replaced by one diode since any one of them would suffice to clamp the line to zero. Similarly, the pairs of diodes on the 2^1 and 2^{-1} lines could be reduced to one. So we can reduce the number of diodes required by a factor of N for N states. The treeing method requires

$$\sum_{1}^{N} 2^N = \text{Number of Diodes} \qquad \textbf{(22.2)}$$

Using diode treeing, a six-stage matrix would require $2^1 + 2^2 + 2^3 + 2^4 + 2^5 + 2^6$ or 126 diodes as compared to 384 for either a straight diode matrix or a diode gate system.

There is one large disadvantage of the tree method. As the number of counts increases, the current carried by the diode clamps increases. In the example given, notice that the 2^2 and 2^{-2} line diodes handle four times as much current as each diode in a straight matrix. Figure 22-3 shows the tree connections for a practical diode matrix.

The diode matrix translation network can be thought of as a code-operated multi-position switch. For each code, one line is actuated. Referring to figures 22-2 and 22-3, notice that for binary number 011, diodes at 0 and 01 activate the line. They could also activate the 010 line with the diode at 01 (figure 22-2). This process expanded is the idea of matrix coding and decoding.

Let's suppose that the codes are stored in a four-bit shift register. The shift register FFs would feed the 2^0, 2^1, 2^2, 2^3, and 2^{-0}, 2^{-1}, 2^{-2}, 2^{-3} inputs. These inputs are referred to as octal numbers. The FF has a total of

16 output lines, representing binary and decimal numbers up to 16 rows and 8 columns (which is called a rectangular diode matrix). The binary circuits feeding the octal inputs have both Q and $\overline{Q}$ outputs. When the binary FFs are in proper sequence, the correct lines are fed to give the binary code to match. This system works well in both directions. Depending on the disposition of inputs and outputs, the matrix will either encode or decode.

By now you should begin to realize that the logic equivalent of a matrix is a multi-input AND/OR gate (one AND/OR gate for each decimal number to be encoded or decoded).

In a decimal-to-binary converter, the right most bit must be a 1 for the decimal numbers ending in 1, 3, 5, 7, 9, and a zero for all the others. The binary output for the right most bit, as seen in figure 22-4, is the output of a five-input OR gate. The other bit positions can be broken out in the same manner. By closing the switch at 9, the output will produce its binary equivalent 1001.

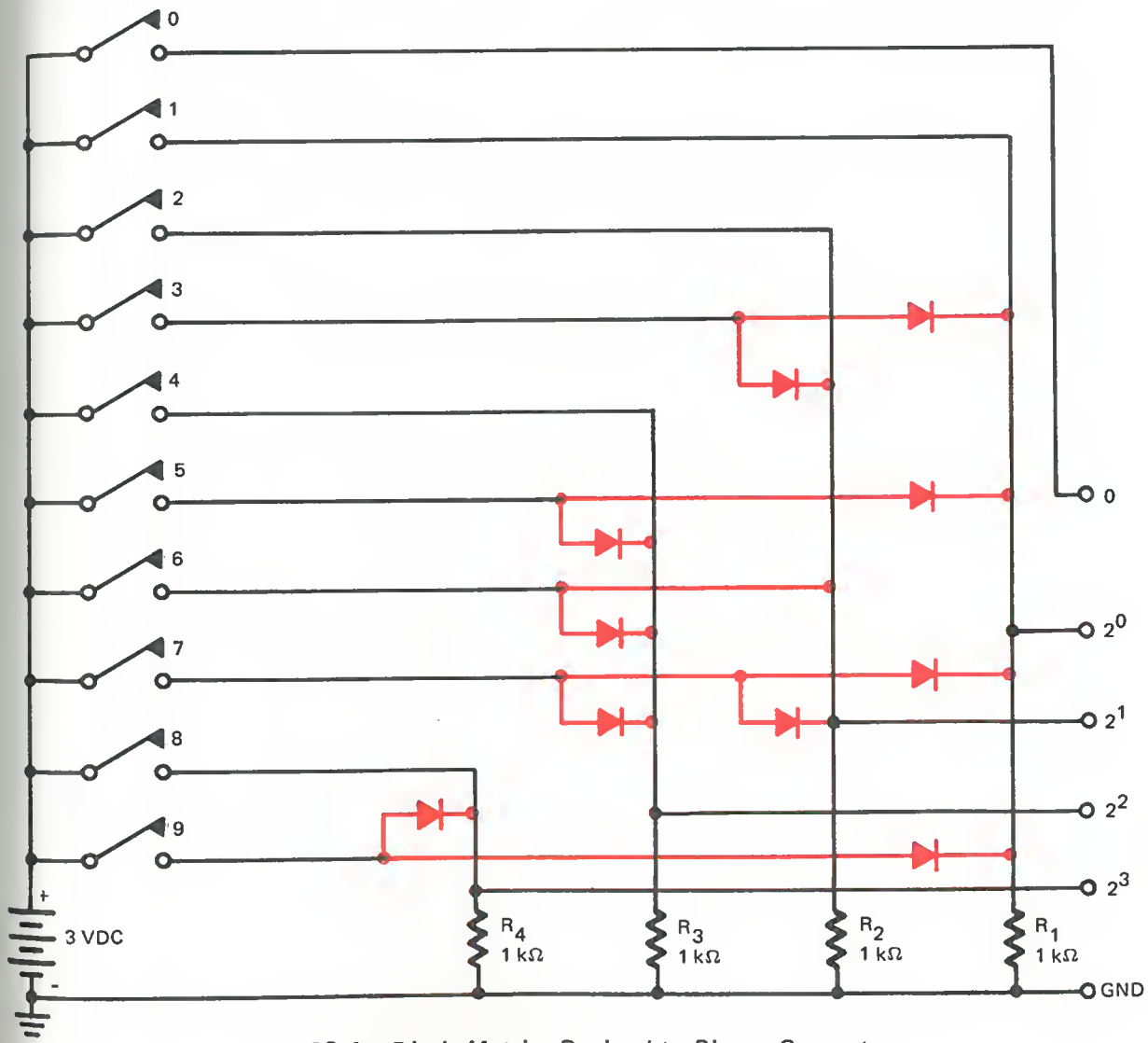


Fig. 22-4 Diode Matrix, Decimal-to-Binary Converter

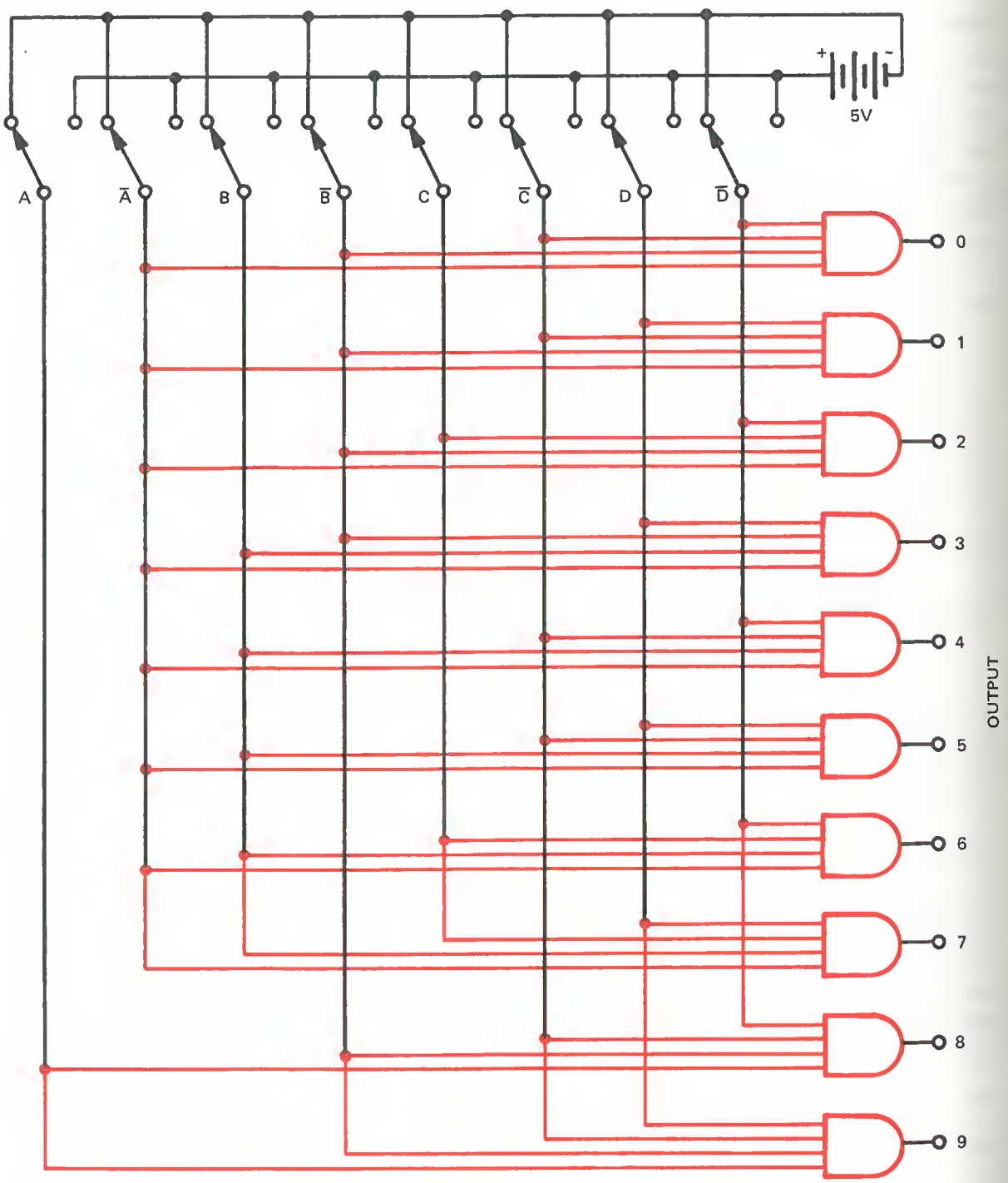


Fig. 22-5 Binary-to-Decimal Converter

Just as OR gates are used for converting from decimal to binary, AND gates are used to convert from binary to decimals. Figure 22-5 shows a binary-to-decimal converter.

Each binary bit position is represented by two lines. The one line or the zero line is energized when the bit value is to be expressed. The binary number five would call for $\overline{A}$, B, $\overline{C}$, D lines to be energized by the shift register or input binary FFs. All nonenergized lines, in this case, A, $\overline{B}$, C, $\overline{D}$, would be clamped to ground potential by a diode or transistor gate.

Diodes are not the only semiconductor devices used in matrix circuits. Actually, any on-off switching device can be used in the construction of a matrix. A check value could substitute as a diode or a gate value for a gate. The input to the matrix could be any number of electromechanical or fluid flow devices.

MATERIALS

11 Diodes, type 1N34 or equivalent
9 SPDT normally-closed switches
1 Oscilloscope
1 VOM or FEM
1 DC power supply (0–40V)
1 Breadboard
4 1 kΩ resistors, 2W

PROCEDURE

1. Construct the experimental circuit shown in figure 22-4.

2. Measure the voltage of the power supply and energize the circuit.

3. Measure the output voltage across each of the 1kΩ resistors for the 9 switches, closed one at a time. Record your results in the data table and calculate the current for each value.

4. With an oscilloscope or VOM determine the voltage level for outputs of 1 and 0.

5. Using a VOM or oscilloscope, determine the binary equivalent of the decimal numbers 0 through 9.

6. Sketch the expanded diode matrix for a decimal-to-binary converter of the type shown in figure 22-4 for the decimal numbers up to 16.

ANALYSIS GUIDE. In analyzing these results you should discuss which of the matrices you constructed seemed to be the easiest to work with. Why do you think so? Where in a practical system would you use a matrix?

Switch That is Closed	0		2^1		2^2		2^3	
	V		V		V		V	I
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								

Voltage Level for 1 = _____

Voltage Level for 0 = _____

Fig. 22-6 The Data Table

PROBLEMS

1. A diode matrix provides 8 outputs. The treeing method is to be used to reduce the number of diodes in the matrix. The current flowing in each output line is 150 mA. What is the current through the diode which is clamping the maximum number of lines?

2. Given a twelve-stage counter, what is the number of diodes using a straight diode matrix? What is the number using the treeing method? Would the treeing method be better?

3. What would normally be used in place of a diode matrix?

experiment 10111 PARITY CHECKING CIRCUITS

INTRODUCTION. Many digital devices employ error detecting circuits of one type or another. In this experiment we will examine a simple single-error detecting circuit and some of the techniques used in its design.

DISCUSSION. It is often necessary to transfer information from one place to another. Whether this transfer takes place entirely inside a computer or spans a distance of several miles, it is not uncommon for errors to occur. There are a great many reasons for these errors and not even the best circuit designer can eliminate the possibility of a failure among the thousands of components used in a modern computer. Therefore, many circuits have been evolved with the capabilities of detecting and sometimes even correcting errors.

In this experiment we will examine design techniques that are often used in the development of a circuit which will detect single errors occuring in four bits of information.

In order to detect these single errors in four bit words, we must include one extra bit which is normally called the parity or check bit. If this parity bit is generated in such a way that an even number of one bits occur in each word, then even parity is generated. If an odd number of one bits occur in a particular word we will know an error is present.

Let's suppose that we need the ability to transfer the B C D equivalent of the decimal numbers zero through fifteen. To do this we will need four inputs to represent the word and one input for the single error detection. Figure 23-1 illustrates the use of an even parity bit to the B C D words.

Notice that for the five variables A, B, C, D and P, there is always an even number of 1s.

Now we are faced with the problem of generating the parity bit P. Since the values of the other four variables determine the value of P, it will be to our advantage to determine a Boolean expression of P in terms of the literals A, B, C and D.

Referring back to figure 23-1, note the column listed "Sum of Products." In this column, the values of A, B, C and D are listed when P = 1. For example, for the decimal number one, P = 1, A = B = C = 0 and D = 1. Therefore, the product term $\bar{A}\bar{B}\bar{C}D$ is listed in the "Sum of Products" column. Since the literals A, B and C were equal to 0, their not values were included in the product term.

Now it is possible to write a Boolean expression which defines all combinations of A, B, C and D for which P = 1. This is done by simply adding (in Boolean form) all the terms in the "Sum of Products" column. In this case, $P = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$.

From this expression a circuit could be designed which would generate P. However, it would be to our advantage to reduce this expression. Therefore, we make use of the

Input →	A	B	C	D	P	Sum of Products ↓
Binary → Equivalent	8	4	2	1	even parity	
Decimal Equivalent ↓	THE B D C WORDS ↓					
zero	0	0	0	0	0	
one	0	0	0	1	1	$\bar{A}\bar{B}\bar{C}D$
two	0	0	1	0	1	$\bar{A}\bar{B}C\bar{D}$
three	0	0	1	1	0	
four	0	1	0	0	1	$\bar{A}B\bar{C}\bar{D}$
five	0	1	0	1	0	
six	0	1	1	0	0	
seven	0	1	1	1	1	$\bar{A}BCD$
eight	1	0	0	0	1	$A\bar{B}\bar{C}\bar{D}$
nine	1	0	0	1	0	
ten	1	0	1	0	0	
eleven	1	0	1	1	1	$A\bar{B}CD$
twelve	1	1	0	0	0	
thirteen	1	1	0	1	1	$AB\bar{C}D$
fourteen	1	1	1	0	1	$ABC\bar{D}$
fifteen	1	1	1	1	0	

Fig. 23-1 Even Parity Words

Boolean identities in the following:

$$P = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$$
$$= \bar{A}\bar{B}(\bar{C}D + C\bar{D}) + \bar{A}B(\bar{C}\bar{D} + CD) + A\bar{B}(\bar{C}\bar{D} + CD) + AB(\bar{C}D + C\bar{D})$$
$$= (\overline{\bar{A}\bar{B} + AB})\,(\bar{C}D + C\bar{D}) + (\bar{A}B + A\bar{B})\,(\overline{\bar{C}\bar{D} + CD})$$
$$P = (\overline{\bar{A}B + A\bar{B}})\,(\bar{C}D + C\bar{D}) + (\bar{A}B + A\bar{B})\,(\overline{\bar{C}\bar{D} + C\bar{D}})$$

We now have the expression of P in its reduced form, and from this, we can design our circuit as shown in figure 23-2.

The distance between the inputs and outputs over which the information is transferred is irrelevant. The important thing about the circuit is to understand that four inputs are fed into the parity bit generating circuit, and the outputs received will be these four inputs plus the parity bit, which can be used to determine if a single error has occurred somewhere in the transmission line.

When these five bits of information are received at the output end, the 1s are counted. Those which have an even number of 1s are accepted as error-free words. Those which have an odd number of 1s are rejected, and the machine takes the course of action previously prescribed by the programmer or operator.

It would have been possible to use an odd parity to accomplish the same results. In fact, an odd parity would have been a better choice because then zero would contain one "1" bit, making possible the distinction of zero from no information.

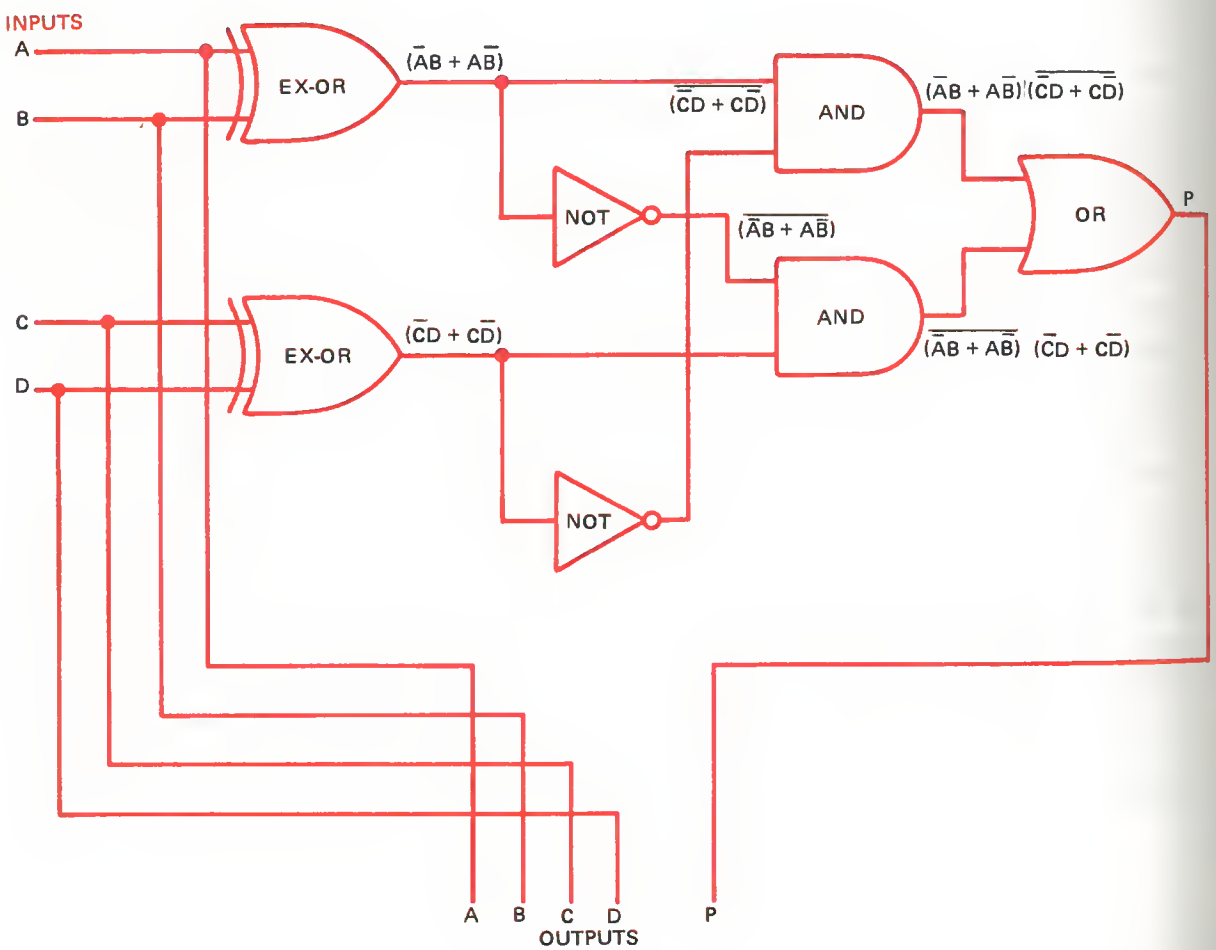


Fig. 23-2 Circuit for Generating the Parity Bit

MATERIALS

1 Oscilloscope
1 DC power supply (0–40V)
10 IC Sockets
10 Dual 4-INPUT NAND/NOR GATE, type SN15830N or equivalent

PROCEDURE

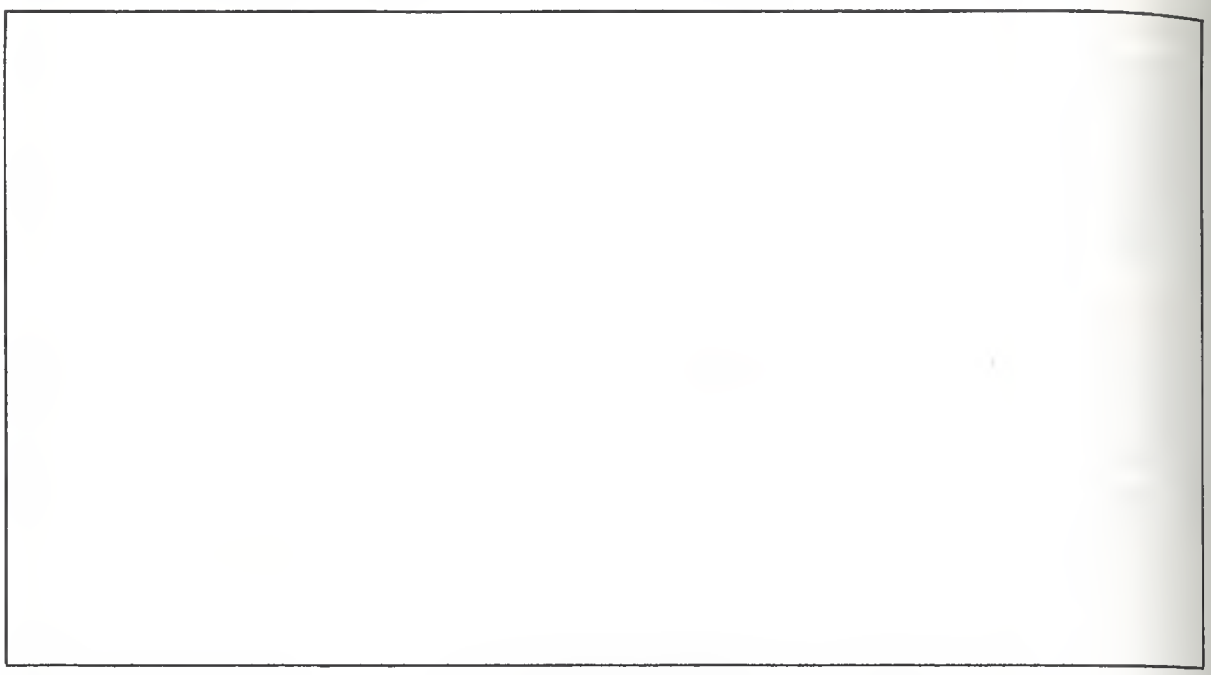
1. Figure 23-2 is composed of 2 EXCLUSIVE-OR gates, 2 NOT gates, 2 AND gates, and 1 OR gate. All of these circuits can be implemented from NAND gates. Draw a circuit diagram of figure 23-2 using only NAND gate circuits. Have this diagram ready for the lab instructor's approval *before* class.
2. Assemble the individual circuits needed and check each one to see that it is operating correctly.
3. Now connect the individual circuits to form the circuit of figure 23-2. Use $V_{in}(1) = V_{CC}$ and $V_{in}(0)$ = ground. Make a truth table to verify that the circuit is working properly.

ANALYSIS GUIDE. In the analysis of your results you should verify that the circuit performed the desired function. Discuss in your own words how single error parity checks can be used in error detection.

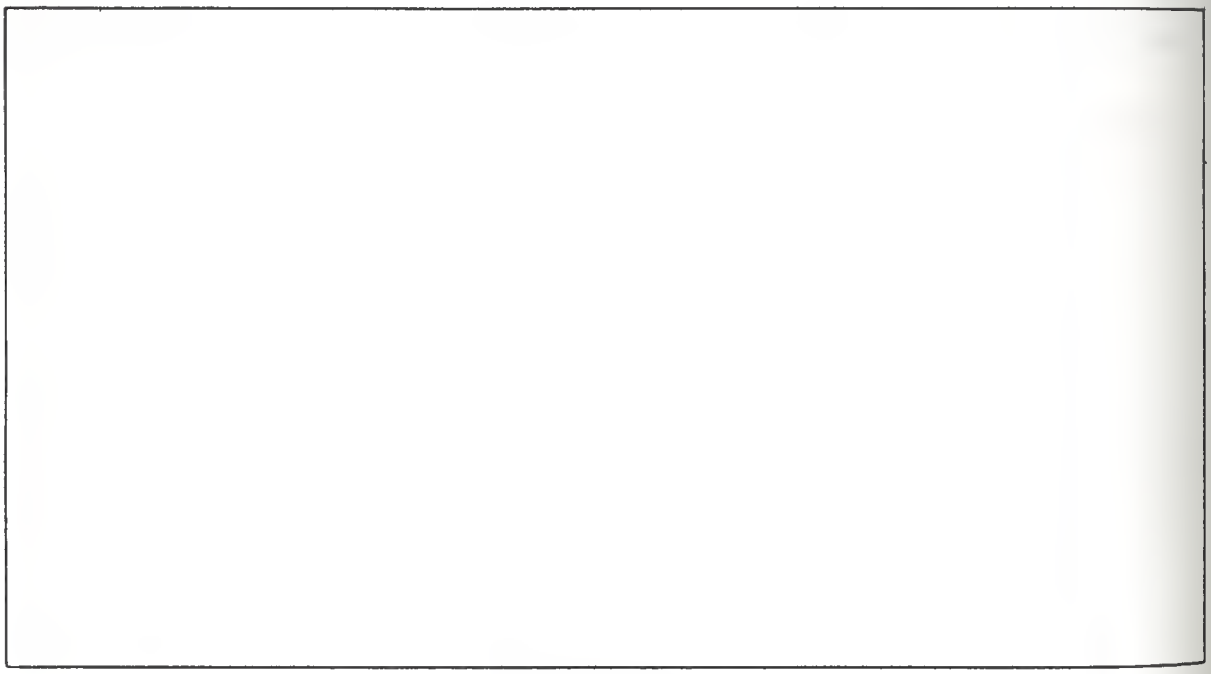
PROBLEMS

1. Make a table similar to that of figure 23-1 using odd parity instead of even parity. The *Sum of Products* column will also change.
2. Use the same method as in the discussion to write a reduced Boolean expression for the odd parity bit of problem 1.
3. Draw a circuit which will generate the expression for the odd parity bit of problem 2.
4. (a) Which of the following output words would be in error if they were received from the even parity circuit of figure 23-2?
   (b) Which would be in error if they were received from the circuit of problem 3?

(1)	00001	(6)	01111
(2)	01101	(7)	11111
(3)	11010	(8)	01000
(4)	01001	(9)	00010
(5)	00000	(10)	01010

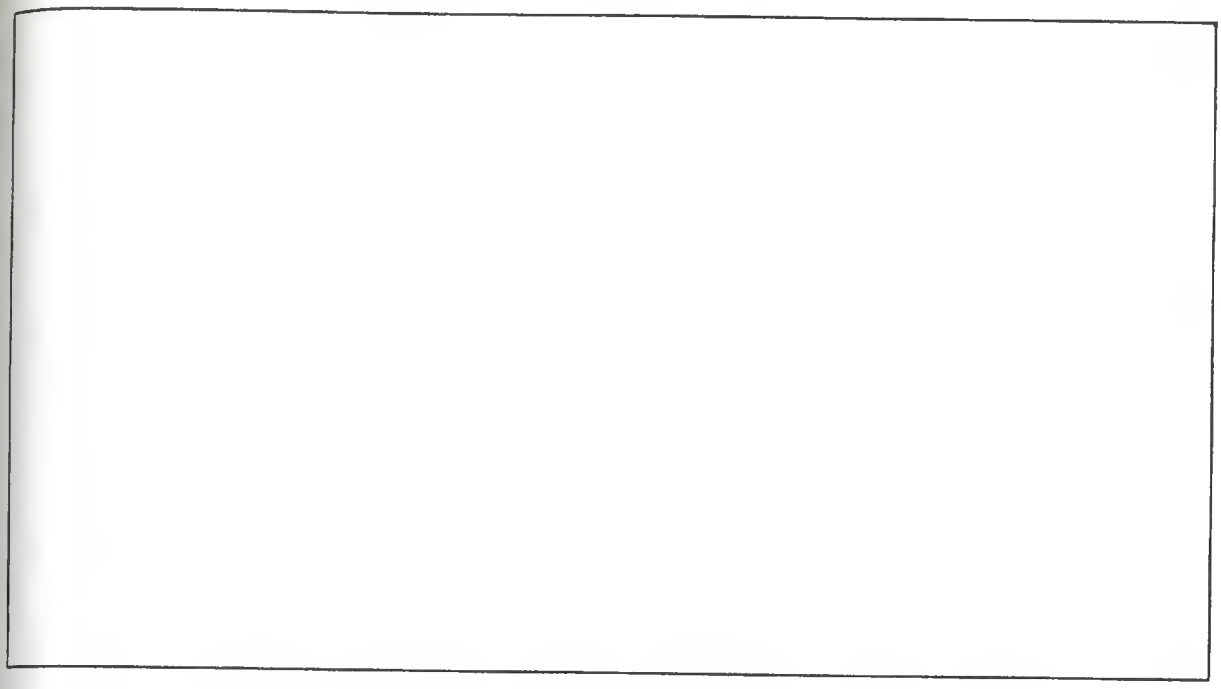


Exclusive-OR Gate

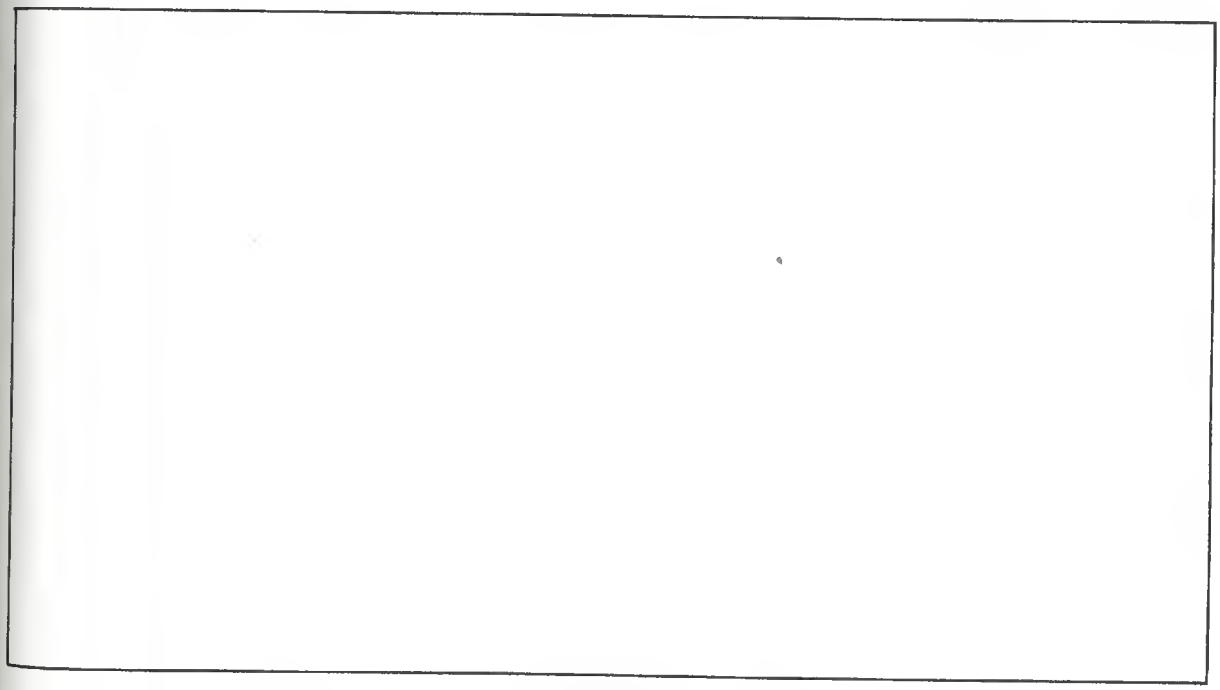


NOT Gate

Fig. 23-3 Gate Diagrams

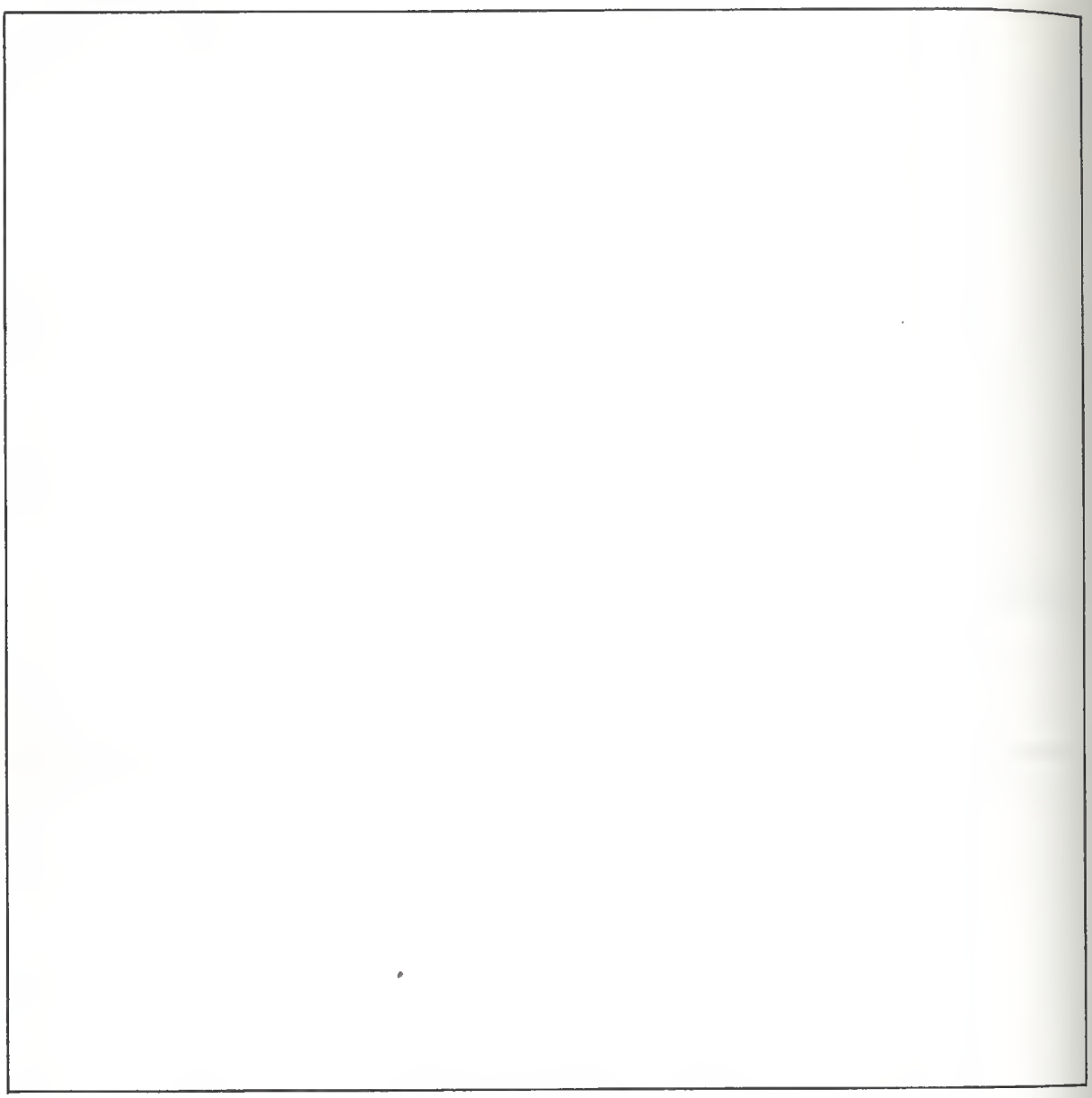


AND Gate



OR Gate

Fig. 23-3 Gate Diagrams (cont'd)



Truth Table

Fig. 23-4 The Truth Table

experiment 11000 INTRODUCTION TO DIGITAL TEMPERATURE CONTROL

INTRODUCTION. The advent of inexpensive integrated circuits has allowed the use of digital control techniques where only analog systems were once economically possible. In this experiment we will examine some basic concepts of digital control.

DISCUSSION. Digital systems involve pulses which may contain information in the repetition rate, pulse-width, amplitude or position of the pulses. These pulses with their attendant information tell the system how to respond. For closed-loop operation, the error signal changes the pulse in such a way that when there is no error the pulse information causes no change in the controlled device. Figure 24-1 is the block diagram of a closed-loop digital servo system.

The clock of figure 24-1 tells the counter *how long* to count the pulses from the variable frequency oscillator. Since this is a fixed time determined by the clock, the number of cycles from the variable frequency oscillator occurring during this time is an indication of the condition of the controlled device. This is because the controlled device is being used to determine the frequency of the variable frequency oscillator.

If the count that accumulates in the counter during a cycle of the clock is the predetermined correct amount, the controller does nothing. However, if the count is wrong, the controller would be activated to correct

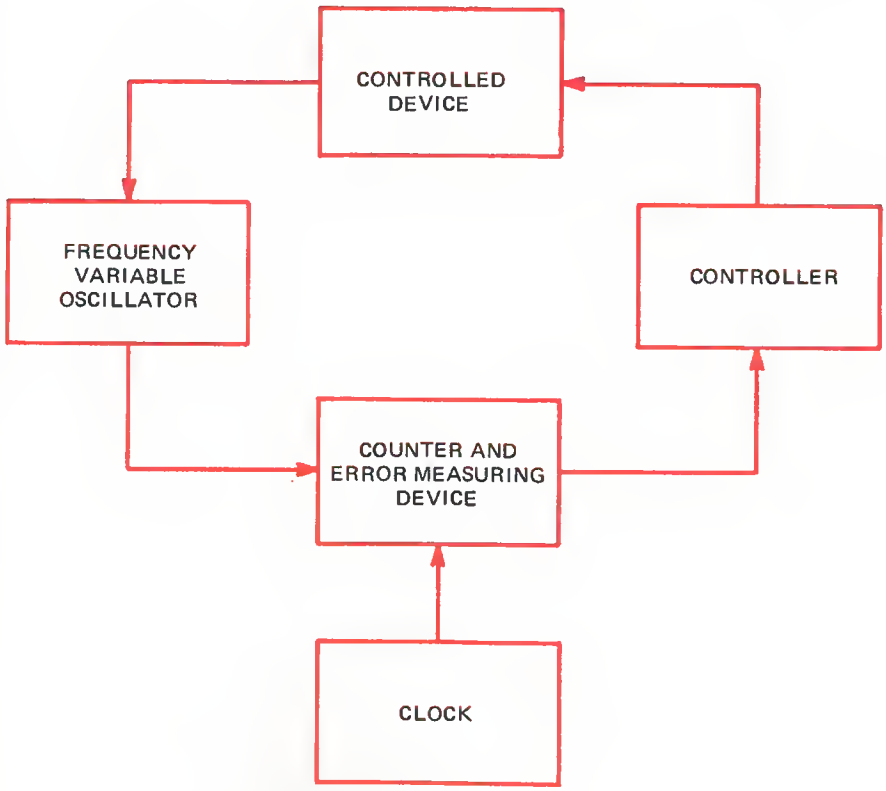


Fig. 24-1 A Digital Control System

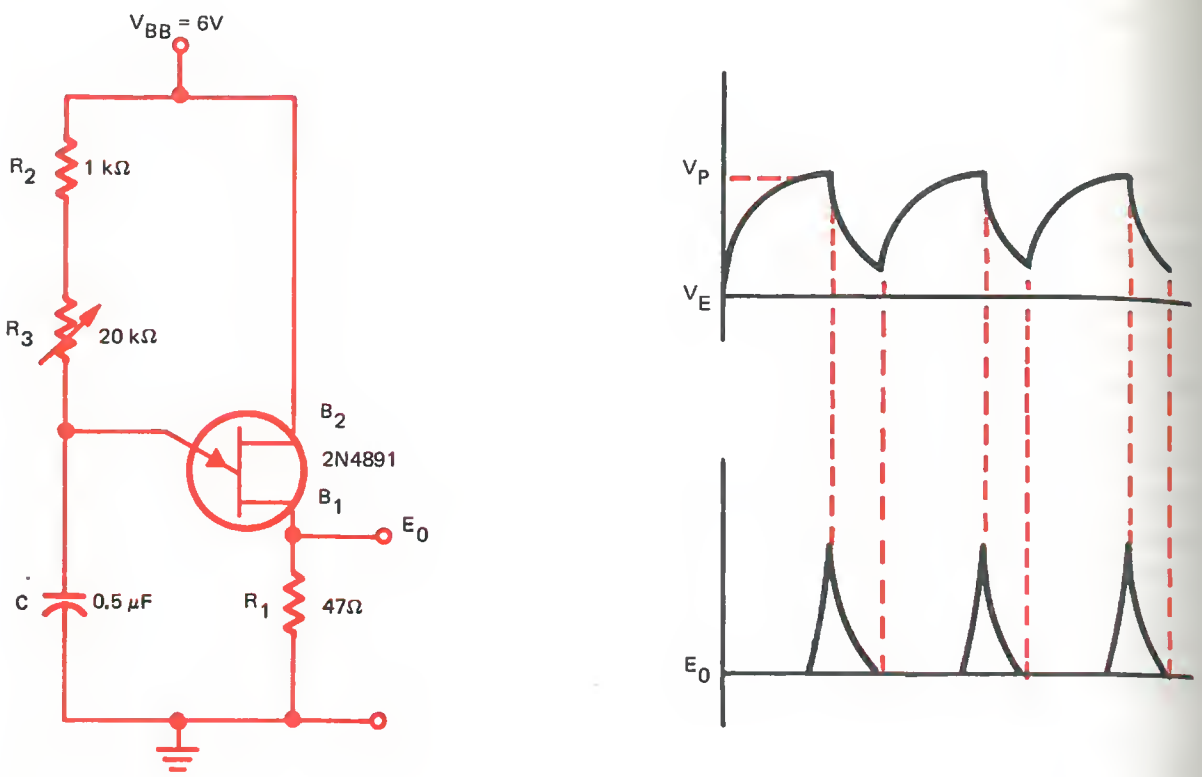


Fig. 24-2 UJT Oscillator

the error which would then produce the correct count, stopping the controller. This general description fits the concept of a closed-loop servomechanism where pulses are used in error sensing.

In this experiment we will be concerned with the variable frequency oscillator.

Figure 24-2 is the circuit diagram of a unijunction transistor (UJT) oscillator. The firing or peak potential, V_p, of the UJT is given by

$$V_p = \eta V_{BB}$$

where η is the intrinsic standoff ratio (a constant for any given UJT which varies from about 0.5 to 0.85 for most devices). V_{BB} is the supply voltage.

Once the capacitor charges to this voltage the UJT "fires", allowing the capacitor to discharge through R_1 and the base one - emitter circuit, generating the output voltage shown. The output frequency, f, is given approximately by

$$f = \frac{1}{R_E C}$$

where R_E is the total emitter resistance. Thus

$$R_E = R_2 + R_3$$

Since R_3 is the variable resistor (could be varied by temperature, light or mechanically), this circuit is the one referred to in the block diagram of figure 24-1 as the variable frequency oscillator.

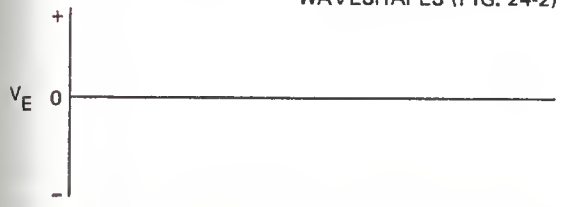
MATERIALS

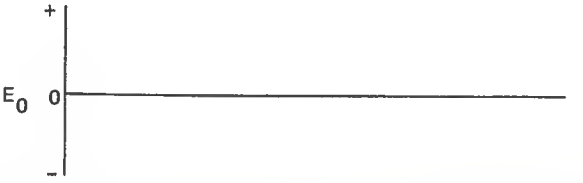
- 2 Potentiometers, 10 kΩ, 2W, linear, or a decade resistance box
- 1 Capacitor substitution box
- 1 UJ Transistor, type 2N4891 or equivalent
- 2 Resistor substitution boxes
- 1 DC power supply (0 - 40V)
- 1 Oscilloscope
- 1 Sheet of graph paper

PROCEDURE

1. Connect the circuit of figure 24-2.
2. Observe and record the waveshapes at the emitter and base one with R_E set approximately at mid resistance.
3. Calculate the approximate frequency for the values of R_E (which is $R_2 + R_3$) shown in the data table.
4. Measure and record the output frequency in pulses per second, PPS at the resistance shown in the data table.
5. Plot a curve of frequency vs R_E and plot both calculated and measured frequencies on the graph.

WAVESHAPES (FIG. 24-2)





R_E	Calculated Frequency	Measured Frequency
1 kΩ		
2 kΩ		
4 kΩ		
8 kΩ		
10 kΩ		
12 kΩ		
14 kΩ		
16 kΩ		
18 kΩ		
20 kΩ		

Fig. 24-3 The Data Table

ANALYSIS GUIDE. Explain why changing R_E changes the frequency of operation and why the measured frequency is different from the calculated value.

PROBLEMS

1. Use your graph and determine the value of the resistance, R_3, for a frequency of 75 Hz.
2. Determine the resistance of R_3 for a desired frequency of 150 Hz.
3. Redraw the circuit of figure 24-2 but show the resistor R_2 as a photocell (photoresistive type) with a resistance of 10k ohms with a given light intensity.
4. What would be the value of R_3 if a frequency of 75 Hz was desired when the photocell resistance is 10k ohms? (Use information from problem 1.)
5. What would be the value of R_3 if a frequency of 150 Hz were desired under the condition where the photocell resistance is 10k ohms?
6. If the light intensity on the photocell in the previous question should increase so that the resistance changed from 10k ohms to 5k ohms, how much would the output frequency change if R_3 were held constant at 5k ohms?
7. Name two other transducers whose resistance change with some physical quantity that might be used in place of the photocell.

INTRODUCTION. An electronic clock is often called the heart of the digital control system. In this experiment we will examine a method of making a clock from logic blocks.

DISCUSSION. A multivibrator is very often used in a digital control system to provide pulses, and as a device to synchronize the overall operation of the system. This synchronizing multivibrator is called the clock. The clock used in this experiment will be made from two NOR circuits.

NOR comes from the combination of the words NOT – OR, in which the OR function is performed then inverted. Remember that the output of a 3-input OR circuit is a 1 when input A or input B or input C is a 1. The truth table of figure 25-1 illustrates the OR function. The output is a 1 when any of the inputs is a 1. Note what happens if you invert the OR. By inversion we mean that when the input is high (a 1) the output is low (a 0) or vice versa. To do this in the table, we change the 1s to 0s and 0s to 1s. This inverted OR function is the truth table for the NOR function. Another way of arriving at the same result is to OR the variables:

$$A + B + C = \text{Output of OR}$$

Then invert them:

$$\overline{A + B + C} = \overline{\text{Output of OR}} = \text{NOR}$$

By Demorgan's Theorem we invert each term and change all ORs to ANDs and vice versa in order to invert a quantity.

$$\overline{A} \times \overline{B} \times \overline{C} = \text{NOR}$$

A	B	C	OR Output	Inverted NOR Output
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

Fig. 25-1 Truth Table for OR and NOR

$\overline{A}$	$\overline{B}$	$\overline{C}$	NOR Output
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
00	0	0	0

Fig. 25-2 Truth Table for a NOR Function

The truth table for this expression is shown in figure 25-2. The $\overline{A}$ column, for example, is attained by changing the A column of figure 25-1 so that the 1s are 0s and 0s are 1s. The output is accomplished by performing the AND operation. Notice that the output is the same as the inverted column of figure 25-1 which demonstrates by induction that

$$\overline{A + B + C} = A' \cdot B' \cdot C' = \text{NOR function}$$

A typical digital control system is shown in figure 25-3 in block diagram form.

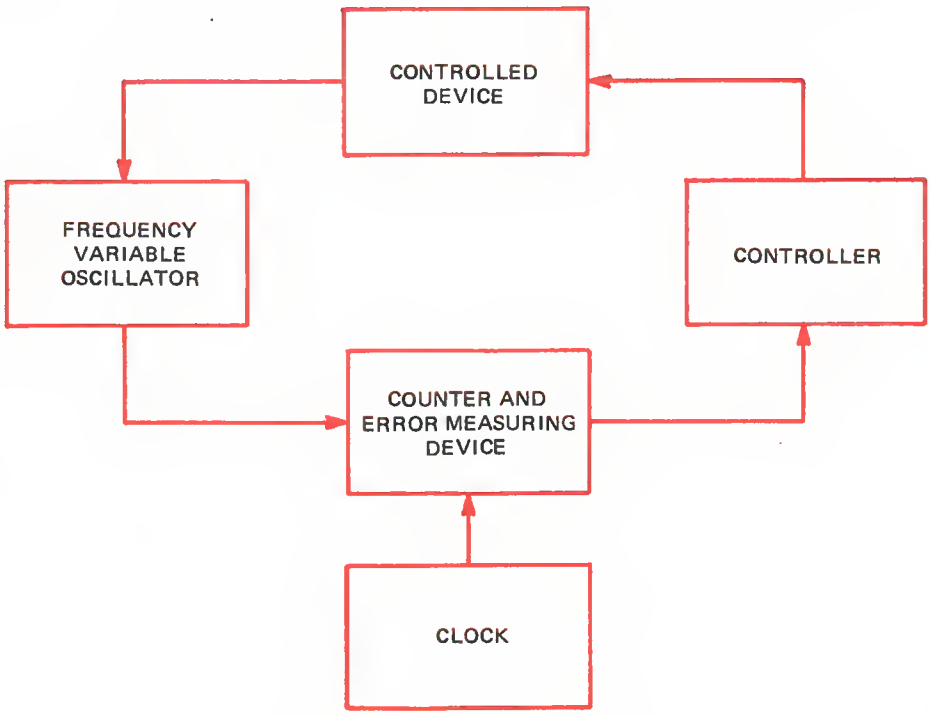


Fig. 25-3 A Digital Control System

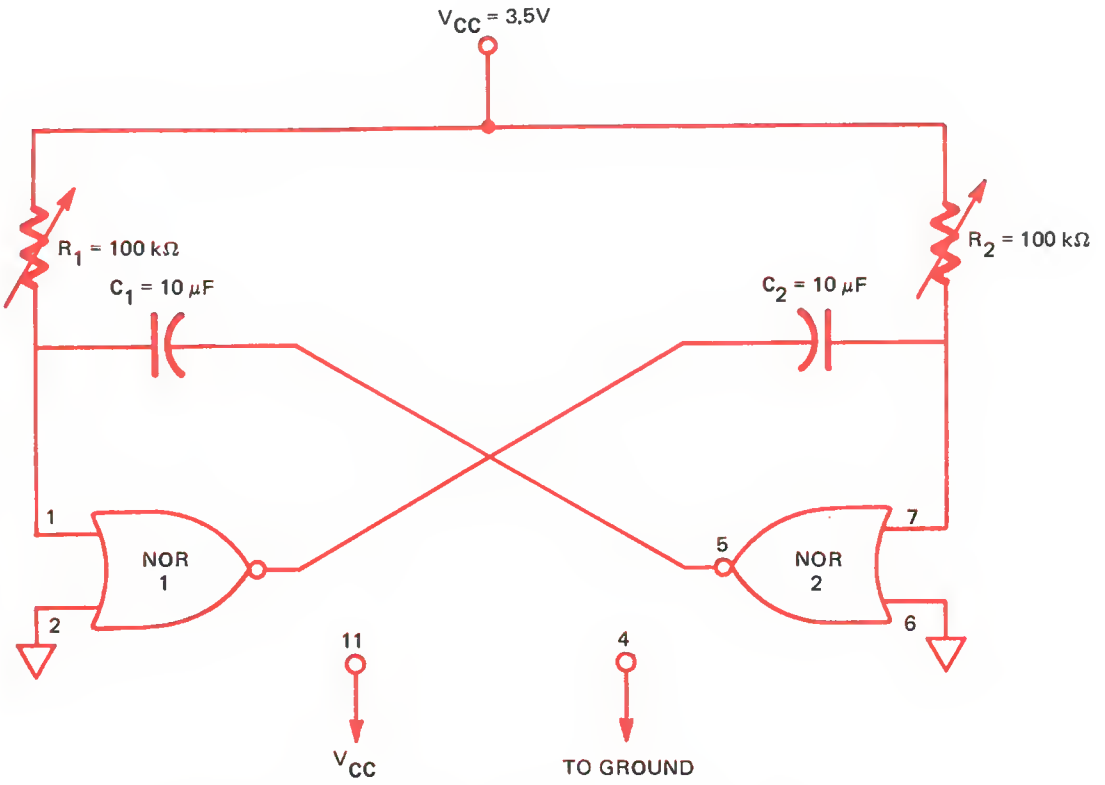


Fig. 25-4 An Integrated Astable Multivibrator Clock

The clock of figure 25-3 tells the counter *how long* to count the pulses from the variable frequency oscillator. Since this is a fixed time as determined by the clock, the number of cycles from the variable frequency oscillator occurring during this time is an indication of the condition of the controlled device. This is because the controlled device is being used to determine the frequency of the variable frequency oscillator.

If the count that accumulates in the counter during a cycle of the clock is the predetermined correct amount, the controller does nothing. However, if the count is wrong, the controller would be activated to correct the error which would then produce the correct count, stopping the controller. This general description fits the concept of a closed-loop servomechanism where pulses are used in error sensing.

You have studied several types of astable (free-running) multivibrators but figure 25-4 may be a version that you have not previously encountered. This one was chosen because the low price of the integrated circuit makes it economical, especially since it contains two other NOR circuits that will be used in the total system to be built later.

The circuit of figure 25-4 is actually a collector-coupled astable multivibrator using the transistors of the integrated circuit. The circuit diagram and integrated circuit layout are shown in figure 25-5. The output frequency, f, is given approximately by

$$f \cong \frac{1}{1.4RC}$$

where the output is a symmetrical square wave.

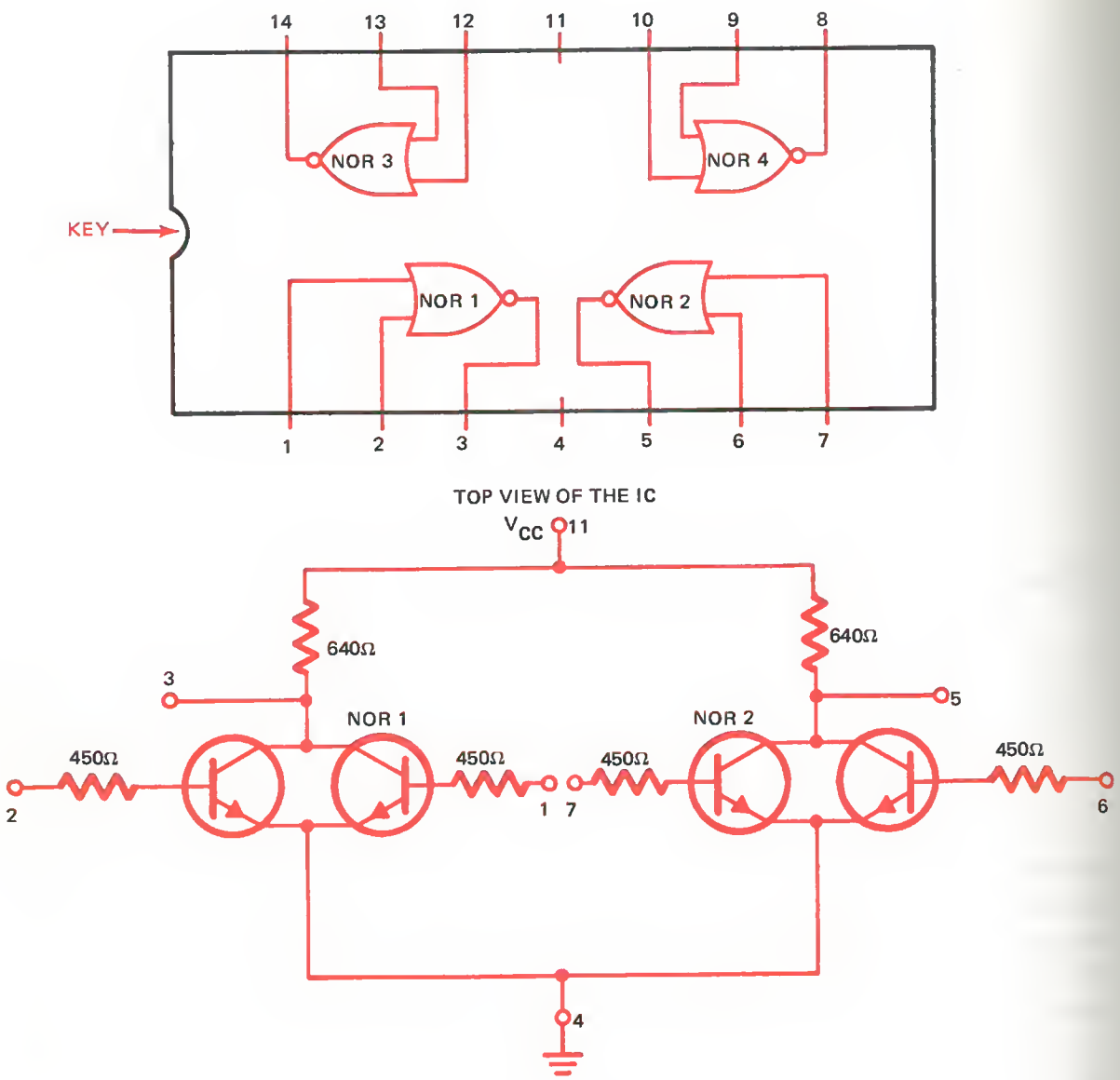


Fig. 25-5 Block Diagram and Circuit of the IC

MATERIALS

1 Quad, 2-input NOR integrated circuit, MC 724P or equivalent
2 Capacitors, 10 μF, 6V
1 DC power supply (0 - 40V)
1 Oscilloscope
2 Potentiometers, 100 kΩ, 1W, linear or a decade resistance box

PROCEDURE

1. Connect the IC so that pin 4 goes to common and pin 11 to the 3.5V supply.

Input A (pin 1)	Input B (pin 2)	Output (pin 3)
0	0	
0	3.5	
3.5	0	
3.5	3.5	

(A)

A	B	Output
0	0	
0	1	
1	0	
1	1	

(B)

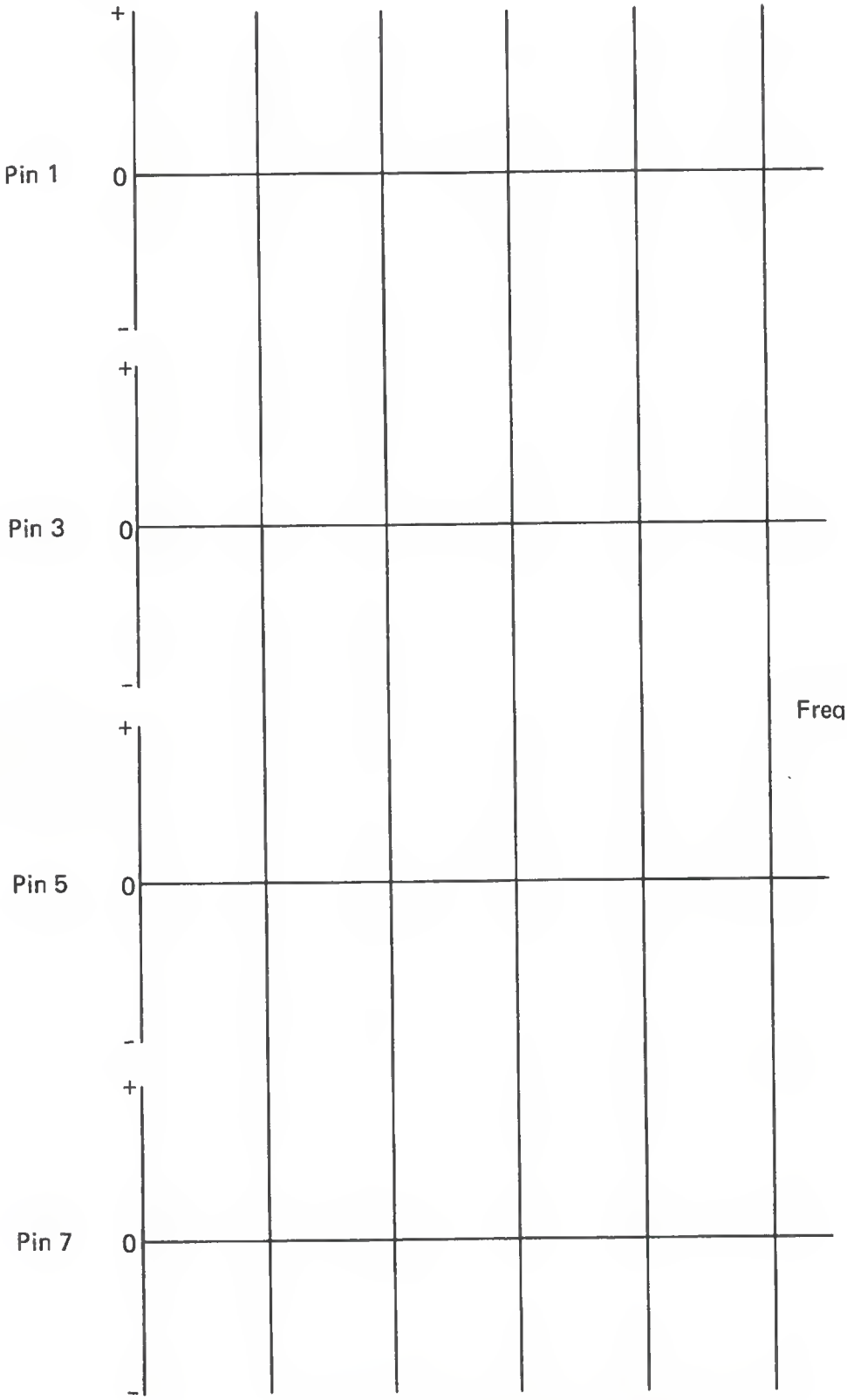
Fig. 25-6 Data for the NOR Logic

2. Complete the data table for the NOR 1 (pins 1, 2 and 3) circuit and record the output voltage in figure 25-6A. Zero voltage means to ground the input
3. Consider voltage less than 1 volt a *zero* and more than 1 volt a *one* and complete the truth table of 25-6B.
4. Connect the circuit of figure 25-4. Set the resistors to 10 kΩ. Be sure pins 11 and 4 are connected to V_{CC} and ground, respectively.
5. Record the output waveshapes at pins 1, 3, 5 and 7 in figure 25-7. Use external sync so that the phase relationship of the waves can be determined.
6. Adjust the potentiometers one at a time and observe the nonsymmetrical output waveform on the oscilloscope.
7. Adjust the variable resistors R_1 and R_2 to get the waveform of figure 25-8. There will be interaction between the settings so it will take considerable adjustment and readjustment to get the desired results. Output can be from either pin 5 or pin 3.
8. Carefully measure the resistance of each potentiometer and record their values in figure 25-8. Be sure to indicate where (from which pin) you got your final desired waveshape.

ANALYSIS GUIDE. In analyzing the results of these data you should consider whether or not they agree with the material presented in the discussion.

PROBLEMS

1. Make a truth table for a three-input AND circuit. Call the inputs, A, B and C.
2. Complement (invert) the output of the truth table of problem 1. What function is represented from input to output?
3. If complements (inverses) of the three inputs are available, show and explain how a NAND circuit may be used to satisfy the OR operation of the original three inputs A, B, and C.

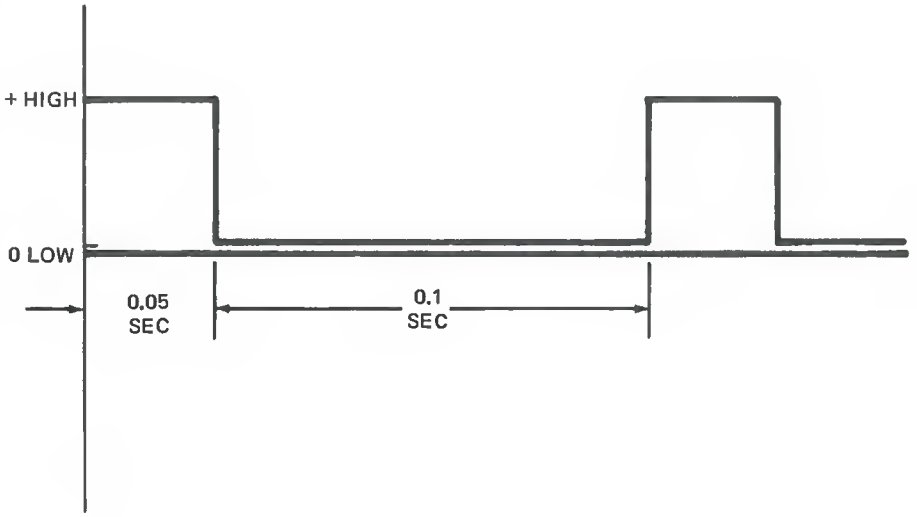


Frequency = _____ Hz

Fig. 25-7 Data Table for Multivibrator

4. Calculate the value of resistors R_1 and R_2 required when $C_1 = C_2 = 1\ \mu F$ to produce an output frequency of 10 kHz.

5. What size capacitors, C_1 and C_2, would be ideal for use with 33 kΩ resistors, R_1 and R_2, if a frequency of 5 kHz was desired?



R_1 = _____ ohms

R_2 = _____ ohms

Fig. 25-8 Data for Nonsymmetrical Output

experiment 11010 MANUAL TEMPERATURE CONTROL

INTRODUCTION. Digital controls are employed in a great variety of industrial systems. In this exercise we will examine the operation of a simple oven, with emphasis on sensing and controlling its temperature.

DISCUSSION. A basic type of digital control can be represented by the block diagram of figure 26-1. This diagram represents a closed-loop digital servomechanism.

The clock of figure 26-1 tells the counter *how long* to count the pulses from the variable frequency oscillator. Since this is a fixed time determined by the clock, the number of cycles from the variable frequency oscillator occurring during this time is an indication of the condition of the controlled device. This is because the controlled device is being used to determine the frequency of the variable frequency oscillator.

If the count that accumulates in the counter during a cycle of the clock is the predetermined correct amount, the controller does nothing. However, if the count is wrong, the controller is activated to correct the error which would then produce the correct count, stopping the controller. This general description fits the concept of a closed-loop servomechanism where a count of pulses is used in error sensing.

This experiment concerns itself primarily with the controlled device. The controlled device will be an oven heated by a 75-watt lamp while the temperature is monitored by a thermistor.

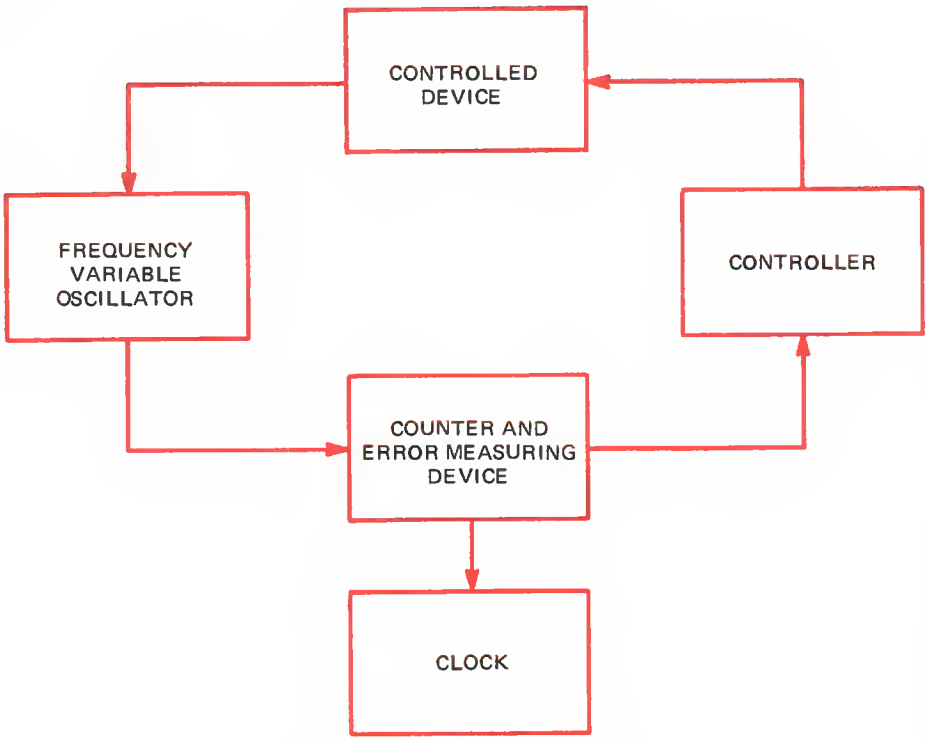


Fig. 26-1 A Digital Control System

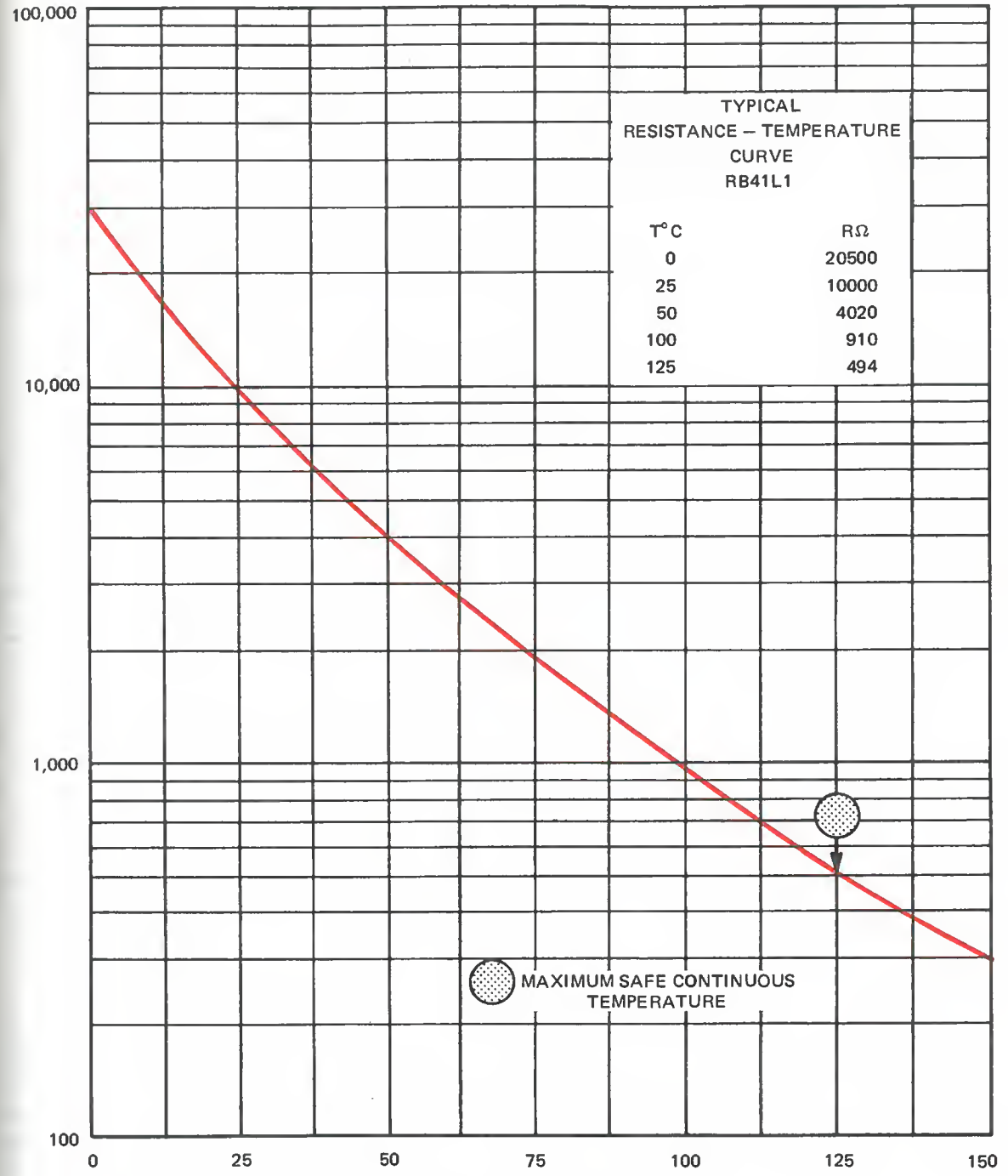


Fig. 26-2 Thermistor Curve

The thermistor to be used in this experiment is a 10k ohm (at 25°C) model that has a negative temperature coefficient of resistance. A negative temperature coefficient means that as temperature goes up, the resistance goes down and visa-versa. Figure 26-2 is the response curve for the thermistor to be used in this experiment.

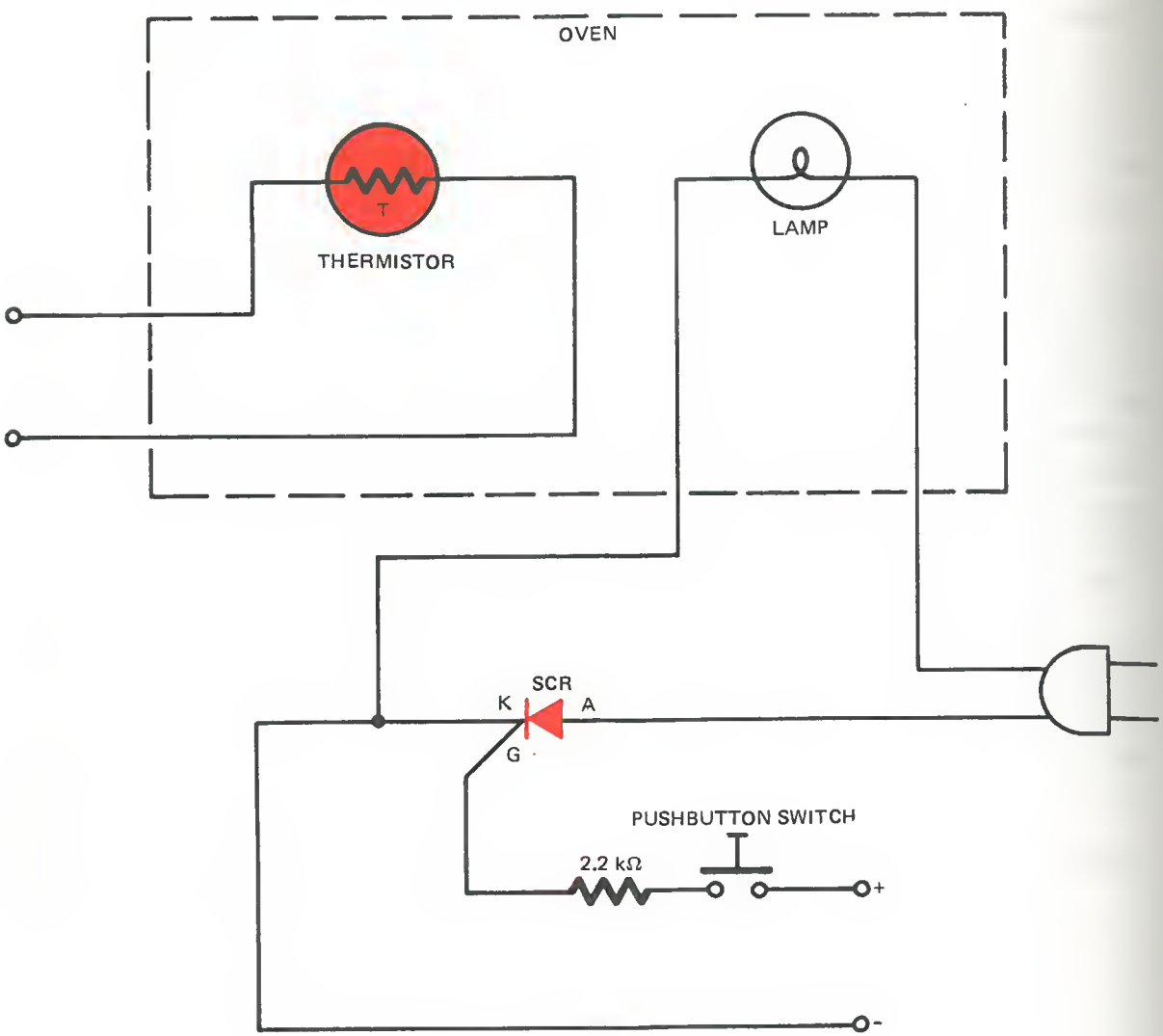


Fig. 26-3 Experimental Setup

The experimental setup is shown in figure 26-3. The thermistor resistance will change with temperature and the temperature will increase while the lamp is lighted. The lamp is turned on and off with the pushbutton switch because the gate is connected to the 3.5-volt supply turning on the SCR. Since the SCR has alternating current applied to the anode-cathode circuit, it recovers every half cycle (when the anode is negative and cathode positive) so the switch will, in effect, turn it both off and on. The advantage of this particular arrangement (instead of the switch being directly in the AC line) is the low switch current. The low control current requirement will allow integrated circuit logic blocks to be used later for control of the light.

The lamp only conducts current for half the time (on one half cycle) but even though the power is down to half, note when you run the experiment that about 70% brightness is realized with half power.

MATERIALS

1 Oven (use a cardboard box such as a shoe box)
1 Lamp, 75W, 115V, with socket
1 Thermistor, bead type 10 kΩ, type RB41L1 or equivalent
1 DC power supply (0 - 40V)
1 Pushbutton SPST switch
1 Resistor, 2.2 kΩ, 1/2W
1 SCR, GE type C22B or equivalent
1 Line cord
1 VOM or FEM

PROCEDURE

1. Connect the circuit of figure 26-3.
2. Push the button and observe that the light comes on.
3. Measure the initial resistance of the thermistor with an ohmmeter and record the value in the space provided in the data table.
4. Use the curve of figure 26-2 to determine the room temperature.
5. Hold the switch on so that the light remains ON for about 10 seconds. Quickly observe the thermistor resistance. Record this value in the data table.
6. Use the graph of figure 26-2 to determine the temperature.
7. Repeat this process for the times listed on the data table.

Thermistor Resistance _____

Room Temperature _____

ANALYSIS GUIDE. Explain the basic operation of the circuit. Explain the effect of the time delay of the thermistor on the results. Also discuss how different lengths of time between the steps in the experiment might affect the thermistor readings.

Time	Thermistor Resistance	Temperature
10 sec		
30 sec		
50 sec		
60 sec		
2 min		
3 min		

Fig. 26-4 The Data Table

PROBLEMS

1. An ohmmeter that uses current to measure resistance and power is I^2R. Explain what effect high ohmmeter (or other) currents would have on the temperature of the thermistor and its resulting temperature.
2. Approximate the curve of figure 26-2 with a straight line. What is the y-intercept? What is the slope?
3. Write an equation for the line you drew in problem 2. The equation for a straight line is $Y = mx + b$ where m is the slope and b is the y-intercept.
4. Explain with the aid of diagrams how the thermistor could be used to control the furnace in your home.
5. Briefly explain how a thermistor connected to the evaporator coils of an air conditioner in your car could be used to prevent icing.

experiment 11011 TEMPERATURE CONTROL COUNTERS

INTRODUCTION. Digital control systems often employ counting as an error detection system. In this experiment we will examine integrated circuit counting and how it can be utilized as an error measuring device.

DISCUSSION. A basic digital control system is represented by the block diagram of figure 27-1. It is a closed-loop digital servomechanism. The clock of figure 27-1 tells the counter *how long* to count the pulses from the variable frequency oscillator. Since this is a fixed time determined by the clock, the number of cycles from the variable frequency oscillator occurring during this time is an indication of the condition of the controlled device. This is because the controlled device is being used to determine the frequency of the variable frequency oscillator.

If the count that accumulates in the counter during a cycle of the clock is the predetermined correct amount, the controller does nothing. However, if the count is wrong, the controller would be activated to correct the error. This would then produce the correct count, stopping the controller. The general description fits the concept of a closed-loop servomechanism where a count of the pulses is used in error sensing.

In this experiment we are going to concentrate on the counter and its application in

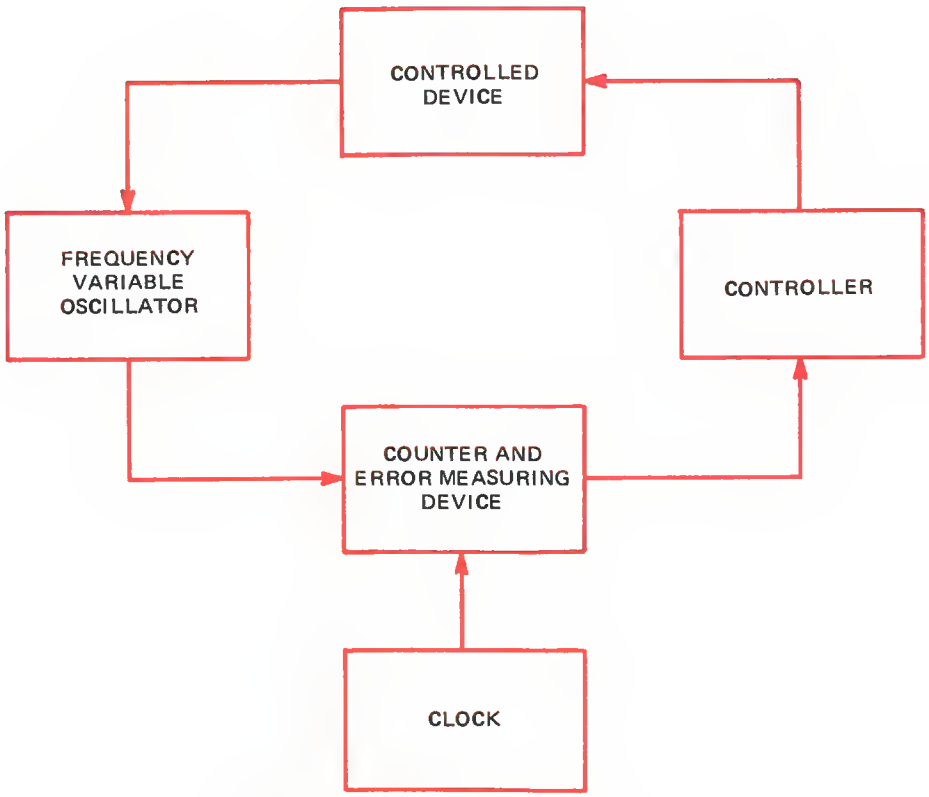


Fig. 27-1 A Digital Control System

BINARY				DECIMAL
2^3	2^2	2^1	2^0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Fig. 27-2 Binary Counting

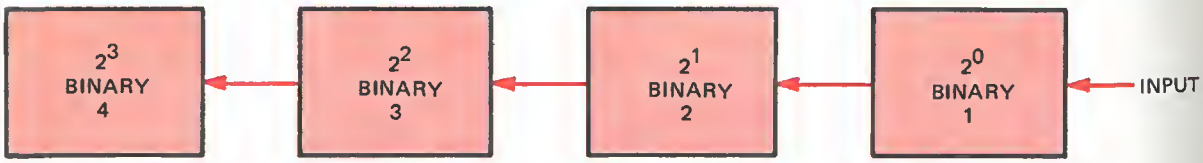


Fig. 27-3 Binary Counter

such a system. We are going to use two integrated circuits with a two-bit binary counter in each one. This will give us a four-bit binary counter. To review the operation refer to the table of figure 27-2.

Each time a pulse comes into the four-stage counter it advances to the next count. To represent this counter with minimum confusion, the *units* digit counter is shown on the right and the 2^3 digit is shown on the left. This makes the count correspond to the table but makes the signal go from right to left, which is reverse to the conventional signal flow in circuit diagrams.

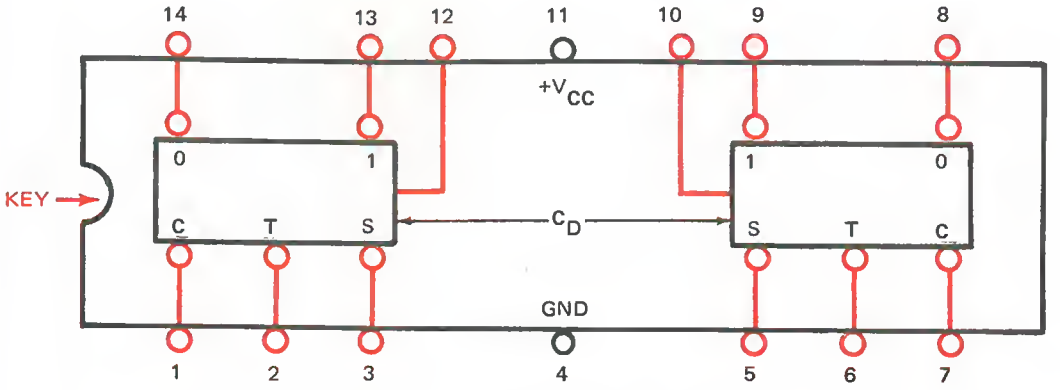


Fig. 27-4 Top View of the MC 790P

The binary counter to be used in this experiment is shown in figure 27-4. You will recognize it as two J-K flip-flops in one package. Pins 10 and 12 are the DC clear pins, C_D.

In order to observe the counting action by manual operation, it will be necessary to use a monostable multivibrator to eliminate false counting caused by switch contact bounce. The monostable remains in its stable condition until pulsed (in the case of this experiment, by pushing a switch), at which time the monostable switches to its unstable state and remains there for a period of time, then returns to its stable condition. The monostable is composed of the two NOR circuits on the left side of figure 27-5. Note that the circuit of figure 27-5 has a signal flow from left to right, which places the units digit on the far left.

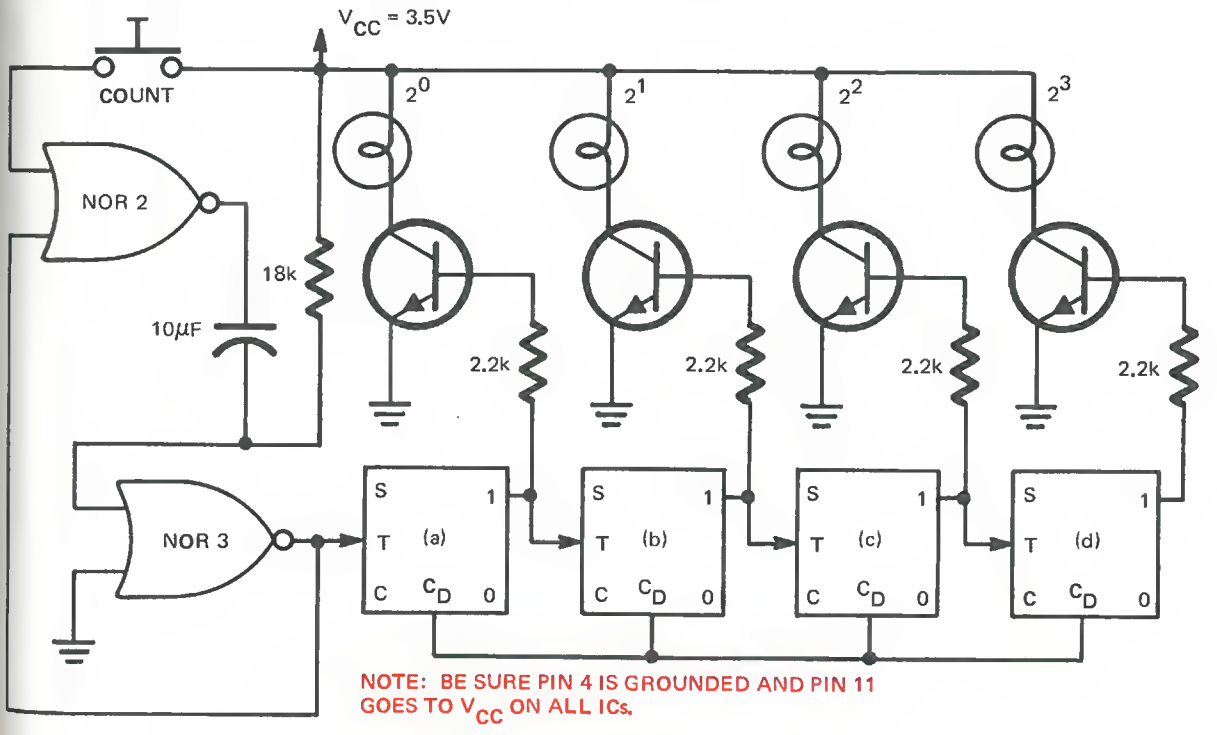


Fig. 27-5 Experimental Circuit

MATERIALS

- 1 Integrated circuit, type MC 790P or equivalent
- 1 Integrated circuit, type MC 724P or equivalent
- 1 Capacitor, 10 μF, 6V DC
- 3 Resistor substitution boxes
- 2 Resistors, 2.2 kΩ, 1/2W
- 1 Switch, pushbutton, normally open
- 4 Lamps, 3V, #48 or equivalent with sockets
- 4 Transistors, 2N3709 or equivalent NPN general purpose type
- 1 DC power supply (0 - 40V)

PROCEDURE

1. Connect the circuit shown in figure 27-5.
2. Apply power and momentarily connect the DC reset line, C_D, to the 3.5-volt supply. All lamps should be out. A lighted lamp is a 1 and an unlighted lamp is a 0, so the first entry line in the data table would be all zeros as shown.
3. Press the count button one time and enter the results in the data table. Remember that the table and circuit are laid out in reverse so that a lamp lighted on the far left enters as a one on the right of the data table.
4. Repeat step three until the first data table is complete.
5. Zero the counter by applying V_{CC} to the C_D line.
6. Connect the 1 output of stage (d) to the S input of stage (a).
7. Press the count button once and enter the results in the second data table.
8. Repeat step seven until the data table is complete. The circuit is supposed to stop counting part way through.

ANALYSIS GUIDE. Explain the circuit operation and tell why the count was different in the second data table from that in the first.

PROBLEMS

1. Draw the block diagram of the four-stage binary counter with the trigger input to the first stage being fed by a 2-input AND. Explain the circumstances under which the binary counter will receive something to count.
2. Suppose one input to the AND gate of problem 1 is being fed a 500-Hz signal, the other input is grounded. What will the counter do?
3. If a pulse of 0.01 sec duration is fed to input 2 while the 500-Hz signal is being fed to input 1, what would the counter read in binary? Assume the counter to be zeroed initially.

4. If the pulse duration of problem 3 were 0.04 seconds, what would the counter have read in binary?

5. Show a connection so that the counter would only count to 8.

6. Show a counter that would stop at 12. Use a 2-input AND circuit to stop the count.

BINARY				DECIMAL
$(d)2^3$	$(c)2^2$	$(b)2^1$	$(a)2^0$	
0	0	0	0	0
				1
				2
				3
				4
				5
				6
				7
				8
				9
				10
				11
				12
				13
				14
				15

Fig. 27-6 The Data Tables

BINARY				DECIMAL
$(d)2^3$	$(c)2^2$	$(b)2^1$	$(a)2^0$	
0	0	0	0	0
				1
				2
				3
				4
				5
				6
				7
				8
				9
				10
				11
				12
				13
				14
				15

Fig. 27-6 The Data Tables (Cont.)

experiment 11100 AUTOMATIC TEMPERATURE CONTROL

INTRODUCTION. Digital servo systems are used to control a variety of industrial processes. In this experiment we will investigate a simplified example of a working digital closed-loop servomechanism.

DISCUSSION. The block diagram of one type of digital control system is shown in figure 28-1.

The clock in figure 28-1 tells the counter *how long* to count the pulses from the variable frequency oscillator. Since this is a fixed time determined by the clock, the number of cycles from the variable frequency oscillator occurring during this time is an indication of the condition of the controlled device. This is because the controlled device is being used to determine the frequency of the variable frequency oscillator.

If the count that accumulates in the counter during a cycle of the clock is the predetermined correct amount, the controller does nothing. However, if the count is wrong, the controller would be activated to correct

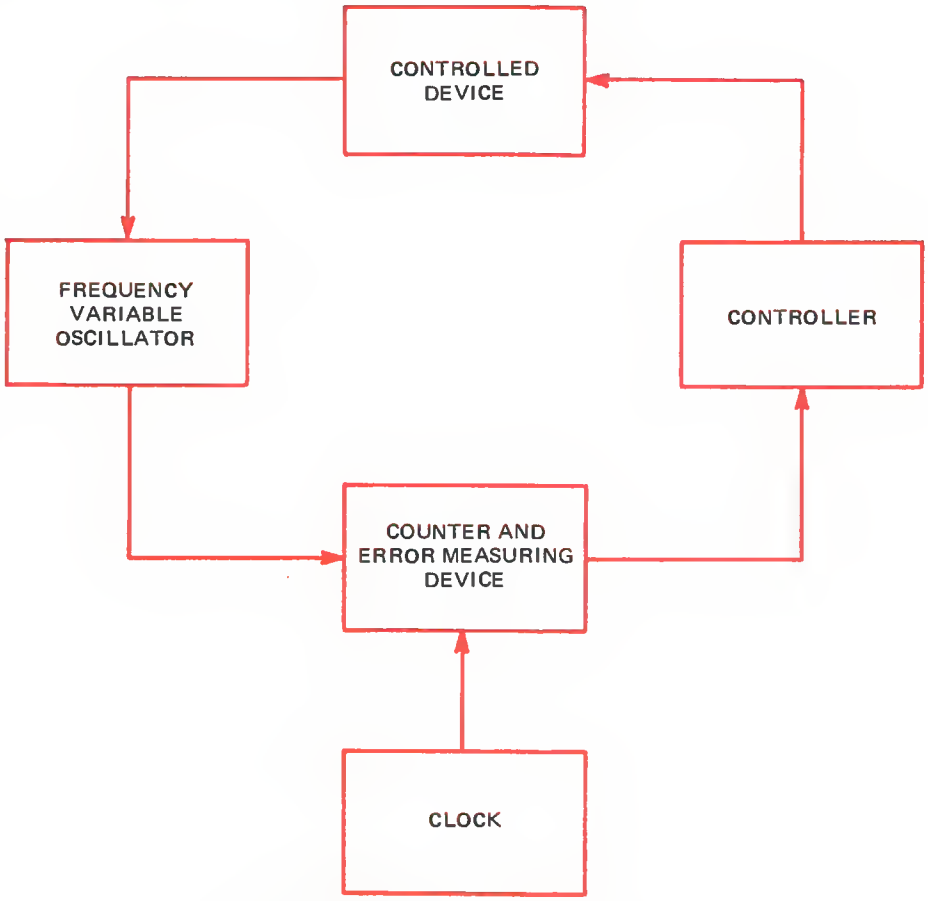


Fig. 28-1 A Digital Control System

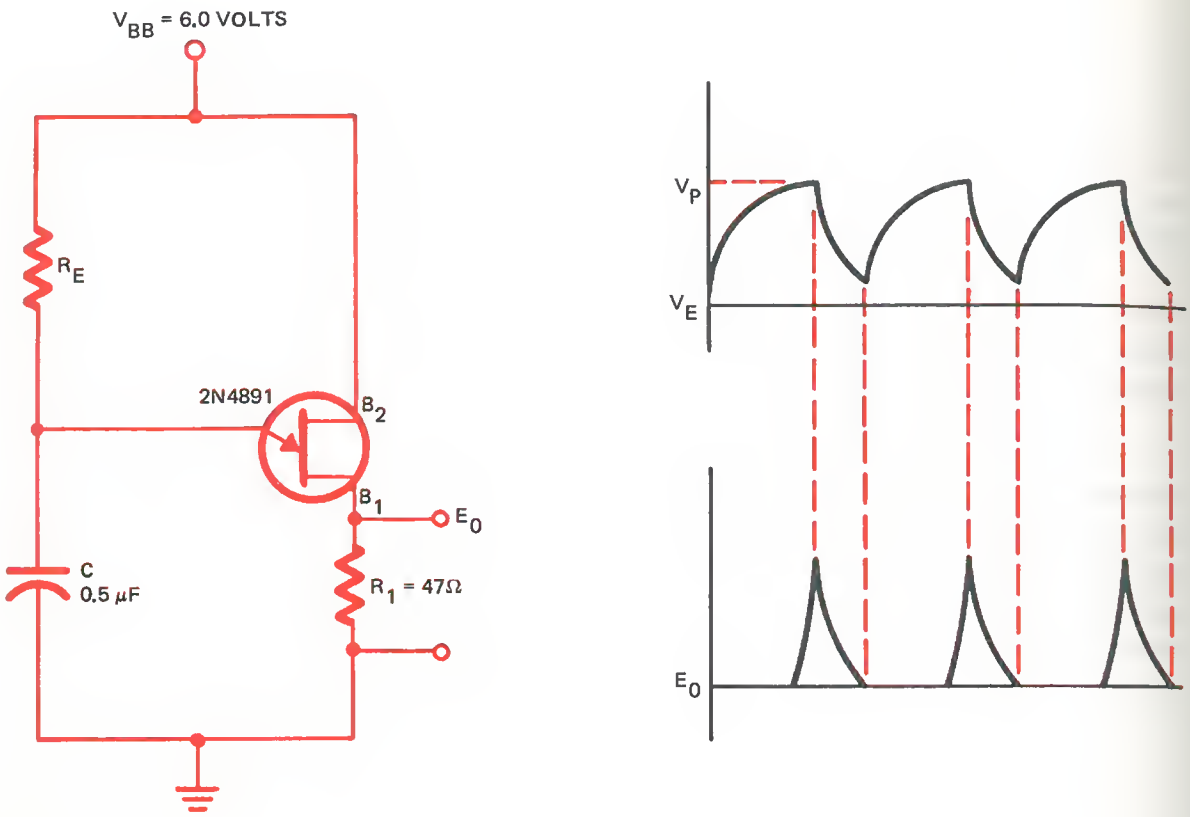


Fig. 28-2 UJT Oscillator

the error which would subsequently produce the correct count, stopping the controller.

A variable frequency oscillator employing a UJT will serve as the pulse source in this experiment. Figure 28-2 shows the circuit diagram that we will use.

The firing or peak voltage, V_p, of the UJT is given by

$$V_p = \eta V_{BB}$$

where η is the intrinsic standoff ratio (a constant for any given UJT which varies from about 0.5 to 0.85 for most devices) and V_{BB} is the supply voltage.

Once the capacitor charges to this voltage the UJT "fires", allowing the capacitor to discharge through R_1 and the base one - emitter circuit, generating the output voltage shown. The output frequency, f, is given approximately by

$$f \cong \frac{1}{R_E C}$$

where R_E is the total emitter resistance.

For the control system that we are going to use, the emitter resistance will be replaced by a thermistor so that as the temperature varies, the frequency of the variable frequency oscillator will change.

The circuit of figure 28-3 is a collector-coupled astable multivibrator. The circuit diagram and integrated circuit layout are shown

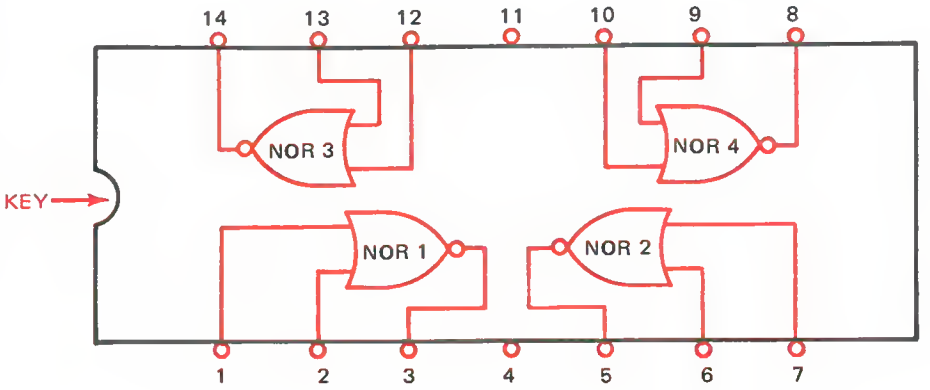


Fig. 28-3(A) Top View of One IC to be Used

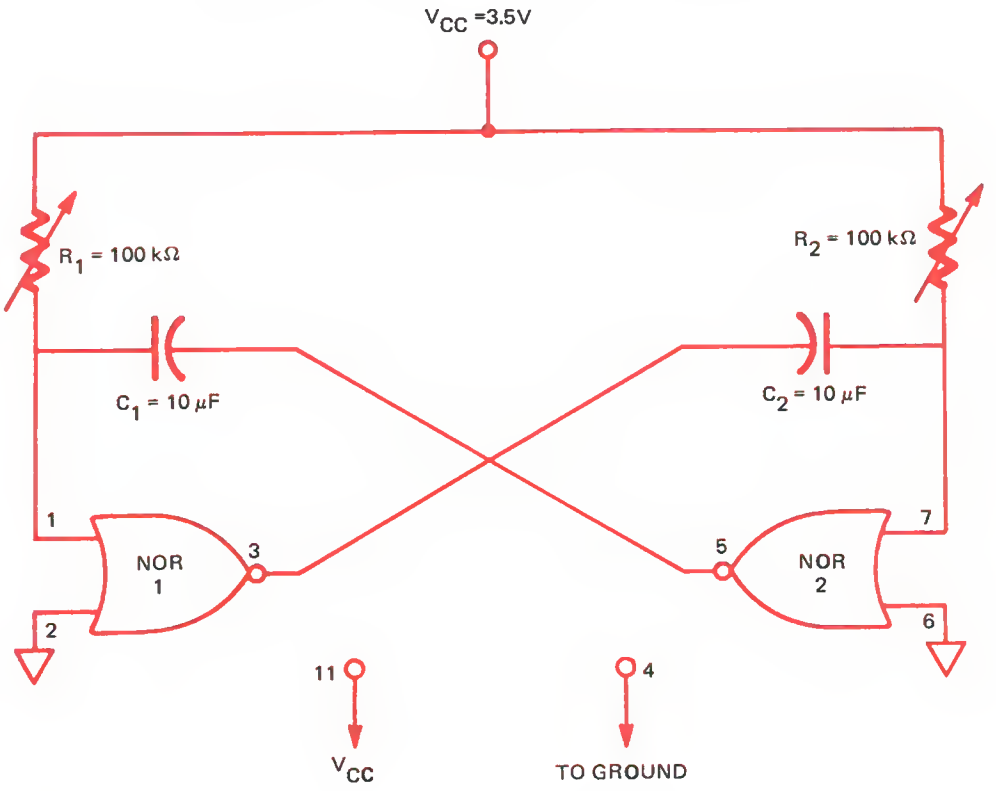


Fig. 28-3(B) An Integrated Astable Multivibrator Clock

in figure 28-3. The output frequency, f, is given approximately by

$$f \cong \frac{1}{1.4RC}$$

where the output is a symmetrical wave.

The desired waveform is one that is similar to the one shown in figure 28-4.

The controlled device in the system will be an oven employing a lamp as the heating element. It is shown in figure 28-5. The SCR controls the lamp which heats the oven and

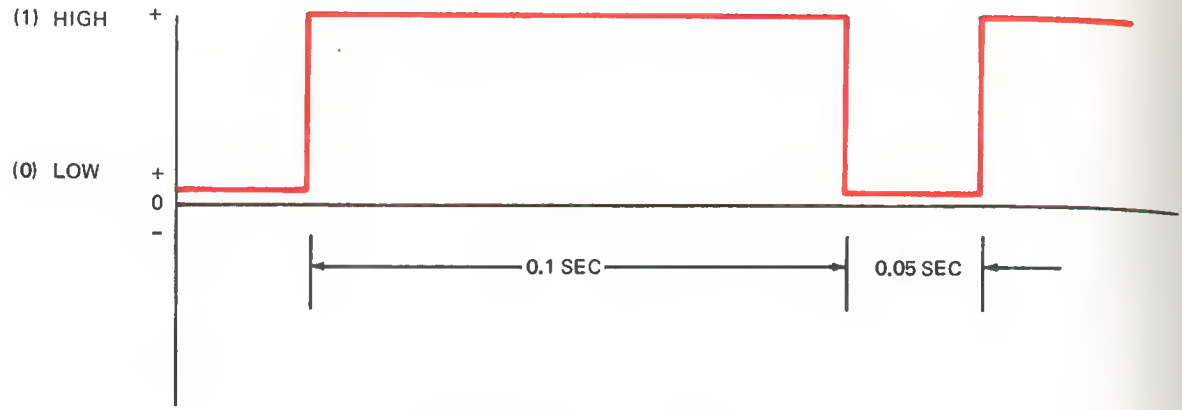


Fig. 28-4 Clock Waveform

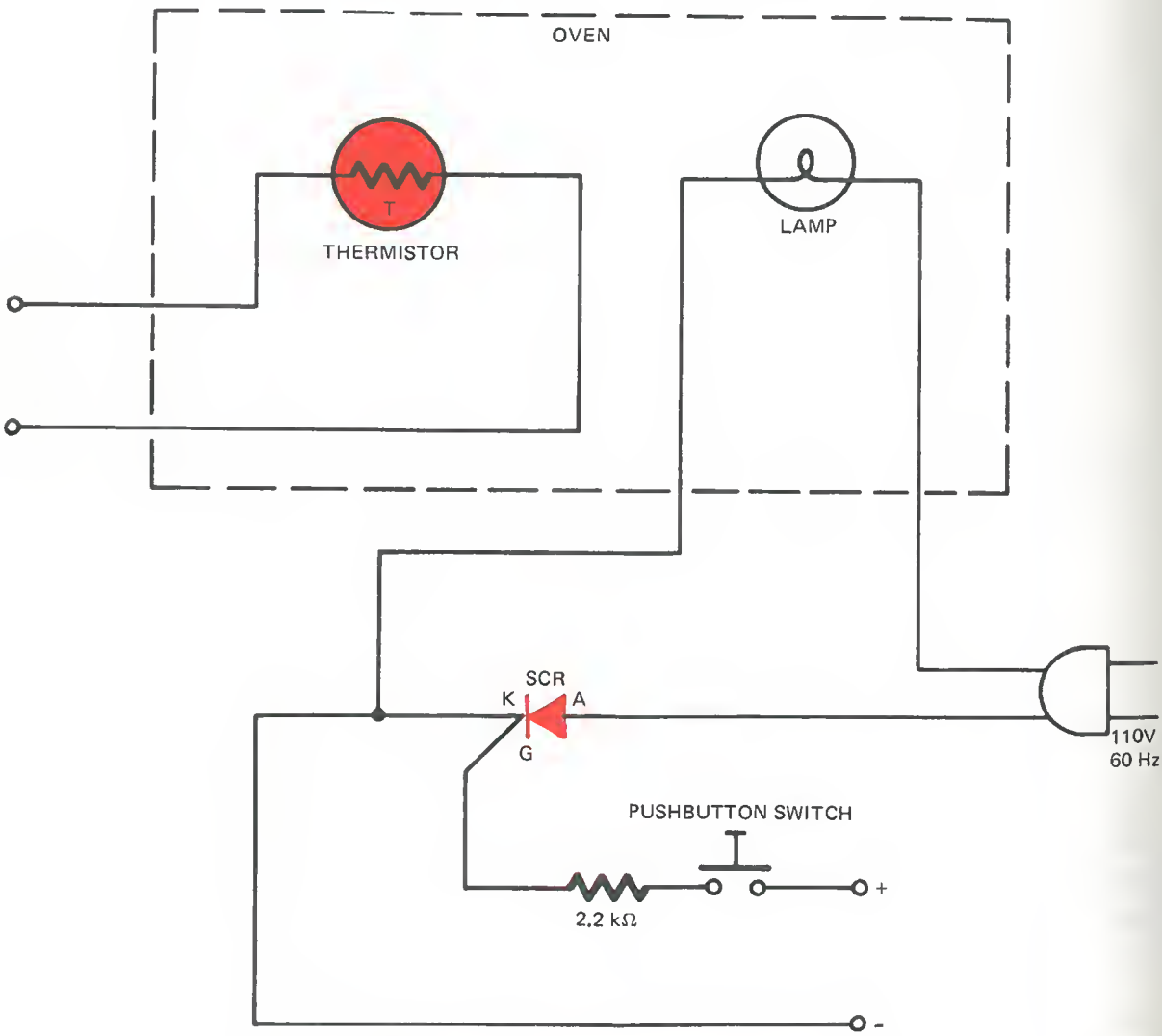


Fig. 28-5 The Controller and Controlled Device

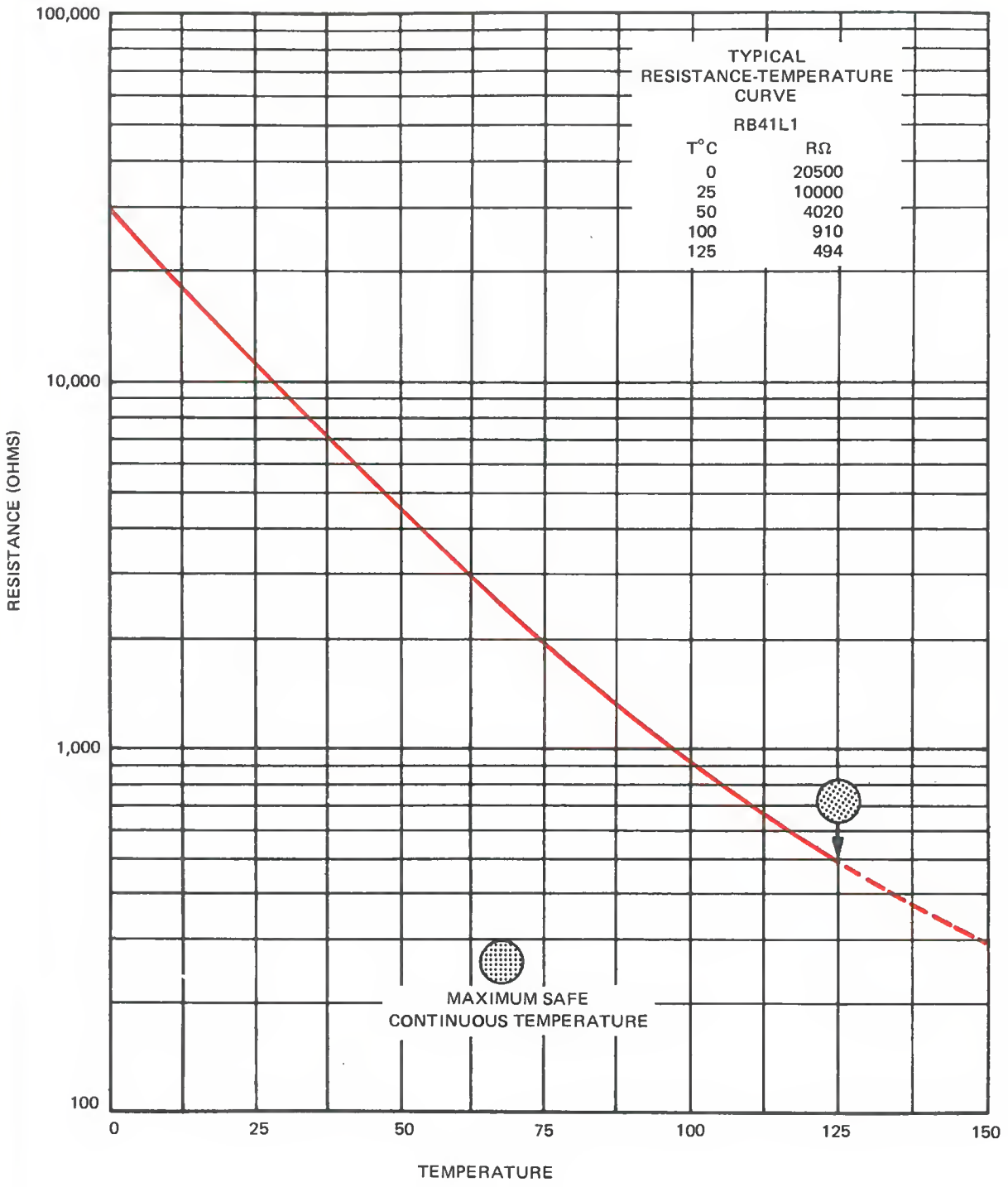


Fig. 28-6 Thermistor Curve

varies the resistance of the thermistor. The thermistor response to temperature is shown in figure 28-6.

The counter that we will use in this experiment is a four-bit counter like the one shown in figure 28-7.

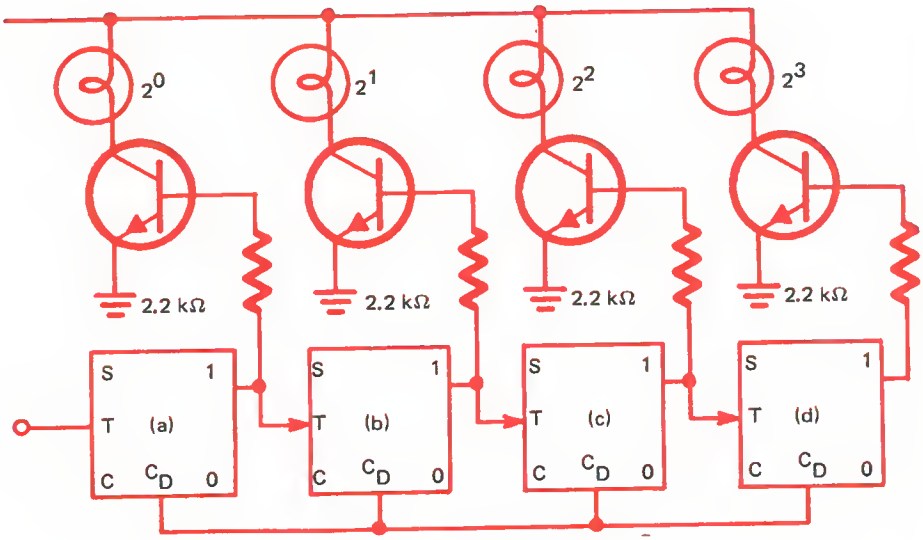


Fig. 28-7 Binary Counter

MATERIALS

- 1 Potentiometer, 10 kΩ, 1/2W, linear, or decade resistance box
- 1 Capacitor, 0.5 μF, 6V
- 1 UJT transistor, type 2N4891 or equivalent
- 1 Resistor, 1 kΩ, 1/2W
- 1 Resistor, 47Ω, 1/2W
- 1 DC power supply (0 - 40V)
- 1 Oscilloscope
- 1 Quad, 2-input NOR integrated circuit, MC 724P or equivalent
- 2 Capacitor substitution boxes
- 1 Capacitor, 0.5 μF, 10V DC
- 2 Potentiometers, 100 kΩ, 1/2W, linear, or decade resistance box
- 1 Oven (use a cardboard box such as a shoe box)
- 1 Resistor substitution box
- 1 Lamp with socket, 75W, 115V
- 1 Thermistor, bead type, 10 kΩ, type RB41L1 or equivalent
- 4 Resistors, 2.2 kΩ, 1/2W
- 1 SCR, GE C22B or equivalent
- 1 Line cord
- 1 VOM or FEM
- 1 Integrated circuit, type MC 790P or equivalent
- 4 Lamps with sockets, 3V, #48 or equivalent
- 4 NPN transistors, type 2N3709 or equivalent, general purpose

PROCEDURE

1. Figure 28-8 shows the waveform of (a) the variable frequency oscillator and (b) the clock, for comparison. They are not shown to actual scale.

2. The (c) part of figure 28-8 illustrates what is desired to go into the counter. The number of pulses let in during time periods 1 and 3 will be an indication of temperature since temperature controls the UJT oscillator. **(Note: This can be accomplished with an AND circuit.)**

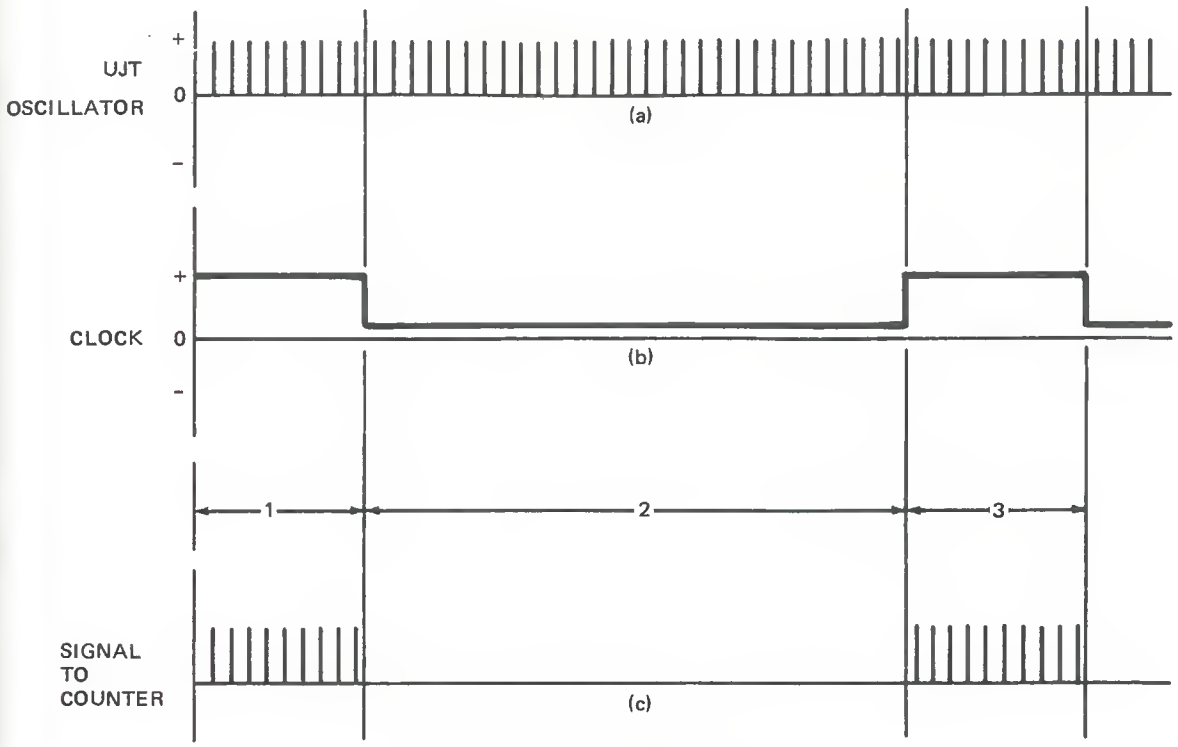


Fig. 28-8 Waveforms

3. Time period 3 is the time for the light to be ON or OFF depending upon the temperature.

4. For this experiment we want to arrange the circuit so that the light will go OFF if the counter reaches a count of digital 8 (binary 1000). This can be accomplished by connecting the 0 output (d) of the binary counter to the gate of the SCR (see figure 28-7). This will turn the SCR OFF when the count of 8 is reached and thus turn the light OFF. If 8 is not reached, the light will remain ON.

5. A positive pulse on the C_D line will zero the counter. Thus, it will be necessary to differentiate the waveform of figure 28-8(b) so that a positive spike at the *beginning* of time periods 1 and 3 will zero the counter.

6. To prevent a higher frequency from counting on past zero, connect the 1 output of (d) of the binary counter to the S input of (a).

7. Use the thermistor curve to determine the resistance at 150°F. Calculate the frequency of the UJT using this resistance as the emitter resistor.

8. Calculate the pulse width needed for time intervals 1 and 3, etc., to let 8 pulses enter the counter at 150°F.

9. Apply power to the clock and adjust for the appropriate time interval. Intervals where the lamp is lighted are not critical in time length.

10. Connect the circuit as in figure 28-9 and measure the temperature in the box after the lamp goes out.

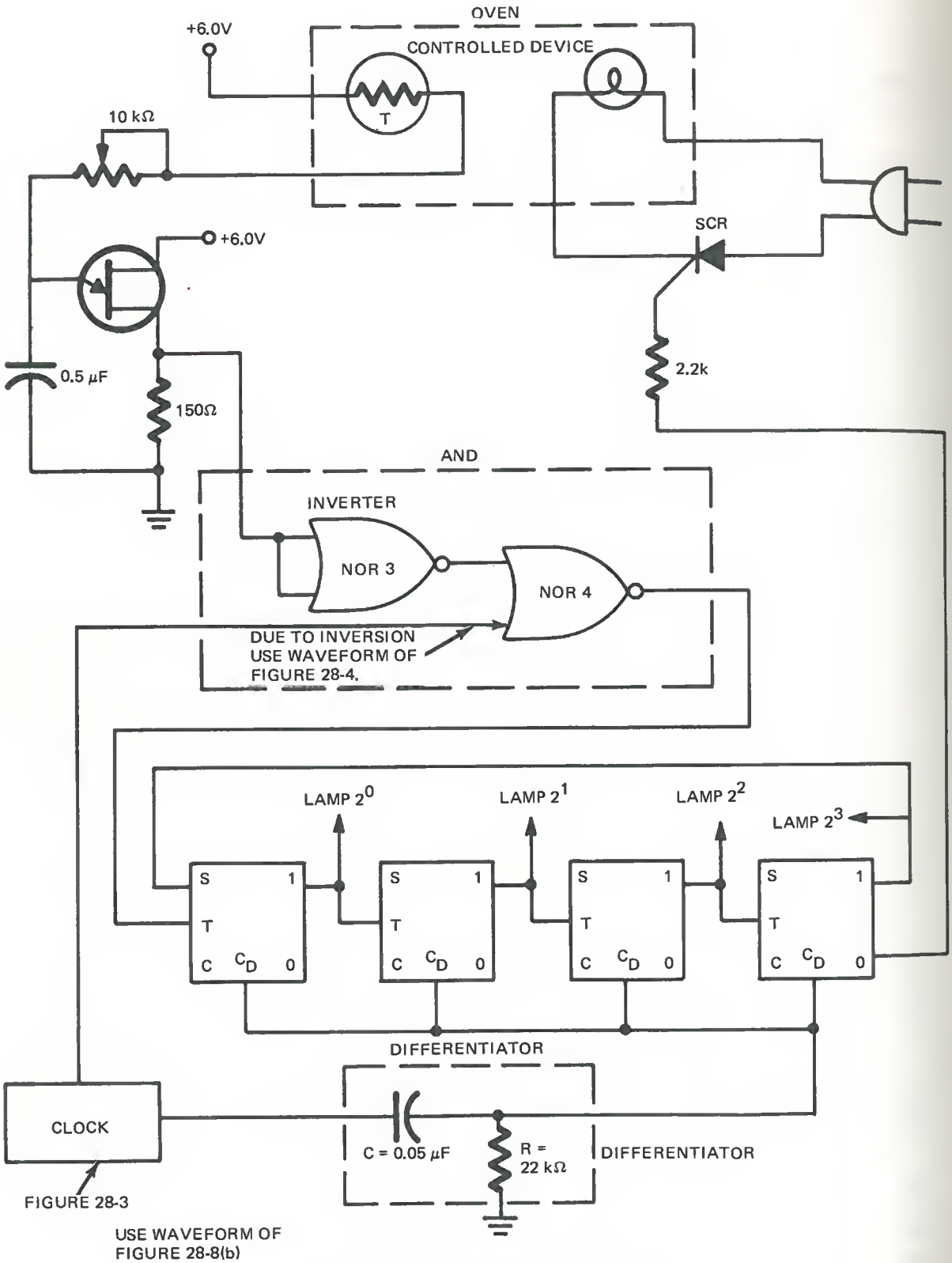


Fig. 28-9 Experimental Setup

ANALYSIS GUIDE. Explain the circuit operation.

PROBLEMS

1. Determine the necessary changes to regulate the temperature at 200° F.
2. Repeat problem 1 for a temperature of 250° F.

experiment 11101 COMPUTER PROBLEM SOLUTIONS

INTRODUCTION. The computer is one of the most frequently encountered applications of digital electronics. In this experiment we will examine some of the elements of the digital computer. We will investigate the function of each element and program the computer to perform a calculation.

DISCUSSION. Solving problems with a digital computer has greatly affected today's world. The speed with which solutions are obtained has enabled space travel to proceed at a fantastic rate. The actual programming of computers has changed in the past few years and each new model has its own characteristics and special applications.

Computer programs can be used to solve simple R-L-C networks and then plot the corresponding time constant curve. Or, the ideal frequency response of an amplifier can be predicted. Programs are available that will indicate at what frequencies an oscillator will function, and what the output waveform will look like. Other applications for computers are in payroll distribution, billing charge accounts, records on checking accounts, medical research, etc.

Each digital computer is a combination of the circuits studied in this course. There are literally thousands of flip-flops and gates in a typical computer. There are four main elements in each digital computer. They are: **1) the control logic, 2) the memory, 3) the arithmetic element, and 4) the input-output equipment.** The interconnection of these four elements comprises the working parts of the computer.

The control logic section is probably the most complex of the four elements. It begins the computations and terminates them when the calculation is completed. Pulse trains of correct amplitude and sequence are generated in the control logic section and thus all the computer's operations are kept in synchronization by the control elements.

The memory elements store data that is to be used in arithmetic operations, and instructions are also stored in the memory. Magnetic cores, tapes, and disks are used simultaneously to store large amounts of data and instructions.

The arithmetic element consists mostly of flip-flops and gates and all the actual calculations take place in this part of the computer. Counters and registers are the most common circuits used in this part of the computer.

The input-output units of the computer are the means by which the operator communicates with the computer. Raw data and instructions are fed into the computer through them, the computations are performed within the computer, and the results are compiled and "returned" to the operator via the output devices. Analog to digital conversations take place in this section and human commands are converted into machine language. Machine language could be fed directly into a computer and the computations performed and recorded, then an operator could convert this language into meaningful data, but the speed at which the computer does this is much faster than that of human operators.

The size of computers varies from small portable models used for special applications to large stationary computers that may be linked with even larger units thousands of miles away which are used for general purpose computations. The baseball player's batting average and the golf tournament standings that are seen each week on TV during play are examples of long distance computer applications. A computer on the West coast may store the information concerning a game on the East coast and the required information is superimposed on the TV screen.

In this experiment we will program the computer to do some problem solving for us. The programs are simple ones but the problem solving ability of the computer will be readily demonstrated. A program using Fortran IV may be written to compute the RC time constant for a known value of R and C.

MATERIALS

1 IBM 1401 computer system (or equivalent)
to include 1401 processing unit, 1402 cardread punch, 1403 printer, 1311 disk storage drive, and 26 printing card punch.
20 Blank cards.

PROCEDURE

1. Punch the program cards to read as shown in figure 29-1. Any mistake in the cards will cause the program NOT to run properly.

```
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
            R = 1 . 0
            C = 1 0 . 0
          5 T = 0 . 0
        1 0 0 U T = 1 0 0 . * ( 1 . - E X P ( - T / R * C ) )
          I F ( T - 5 0 . ) 4 0 , 1 0 0 , 1 0 0
          P R I N T   1 5 0 , T , O U T
      4 0 T = T + 5
          G O   T O   1 0
    1 0 0 P A U S E
          G O   T O   5 .
  1 5 0   F O R M A T   ( 2 F 1 5 . 2 )
          E N D
```

Fig. 29-1

2. Load the program into the card read-punch unit.
3. Get the printout sheet from the printer.
4. Double the value of R and load the new program into the card read-punch unit.
5. Repeat step 3.

ANALYSIS GUIDE. Compare the two computer solutions when R = 1.0, and R = 2.0. What relationship exists between them? Why?

PROBLEMS

1. Calculate values for the voltage across the capacitor when t = 0, 5, 10, 20, 30, 40, and 50 sec; R = 1.0.
2. Plot the computed values and compare them with the computer values. Which value is more correct at $T = 1/2\tau$? where $T = 1\tau$?
3. Explain why you think your answer to problem 2 is correct.

experiment 11110 SUMMARY OF LOGIC OPERATIONS

INTRODUCTION. Digital logic has its own language of symbols and modes of operation. Electronics can be used as the vehicle for performing many logic functions. In this experiment we will review some basic logic devices, symbols, and operations.

DISCUSSION. Logic symbols and diagrams can represent the operation of very complex logic systems in relatively simplified terms. As with any language, a thorough understanding of the terms, symbols and meanings is necessary for effective communication. A set of standard logic symbols has been agreed on, and they will be used herein.

A binary system breaks all information up into groups of two elementary bits. These bits are represented by the two states, on or off. When we are talking about logic states, these are often expressed as 1 and 0. Electronically, the voltage levels do not have to correspond exactly to 0 volts and one volt. For this reason a translation is often made to "Hi" for 1 and "Lo" for zero. Even the meaning of these terms must be defined for a particular system.

The terms Hi and Lo, True and False, 1 and 0 are all relative. The Hi voltage need not necessarily be positive (above ground or zero volts). It is simply higher with respect to the Lo or Off voltage. Logic systems frequently operate at levels between -24 and -12 volts. The Hi voltage here or positive term is -12, which would be designated in the symbols as +. It is also common to encounter a negative logic system where the -24 is True or Hi and +. The presence or absence of current may also be used to designate true or false.

A logic system diagram will usually state that all the logic is either "Positive True" or "Negative True". The choice of words True, False, Hi, and Lo should not confuse you by leading you to think that the true is more significant than the false. Many times the absence of a signal will be more important than the presence of a signal. One other important point is that the Hi, Lo, 1, 0, etc., designations may be used for an individual device or for a complete stage.

It will be easy to remember the logic conversion of 1 and 0 to Hi and Lo if the first letter of Hi and Lo are disregarded. Then they become 1 and 0 for positive logic. Hi = 1, Lo = 0.

In the binary system, bits 0 and 1 are combined to represent numbers. The numbers are each assigned a weight, and each successive bit can be increased in weight by a maximum factor of two. The number of bits required depends on the magnitude of the number to be represented. In the binary number system the weights assigned to successive bits are:

Up	32	16	8	4	2	1	•	1/2	1/4	1/8	1/16	Down
	2^5	2^4	2^3	2^2	2^1	2^0	•	2^{-1}	2^{-2}	2^{-3}	2^{-4}	

Each bit is true or false, and to obtain the number, the weights of all the "True" bits are added. Therefore, the pure binary number for 22.5 is 10110.1000.

Weight	2^4	2^3	2^2	2^1	2^0	·	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Decimal No.	16	8	4	4	2	·	1/2	1/4	1/8	1/16
Binary No.	1	0	1	1	0	·	1	0	0	0

Notice that just as in the decimal system, digits may be added to the right of the point to provide a more accurate number. The decimal point in the binary system is called the binary point.

Input-output tables for either particular devices or for complete stages are called Truth Tables. These tables show the inputs and outputs which are of importance in a particular function. In the symbol system there are four basic types of symbols. These basic symbols are shown in figure 30-1.

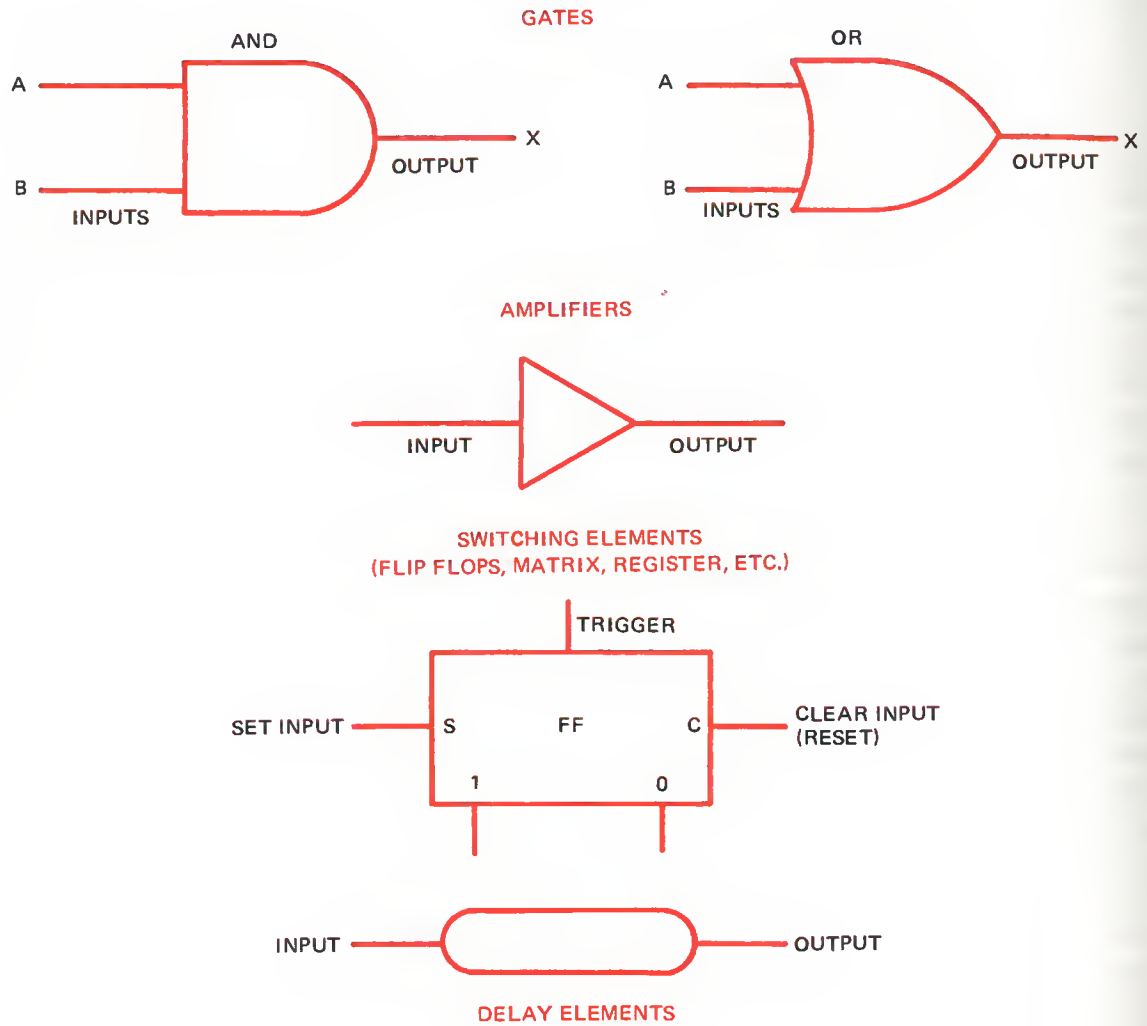


Fig. 30-1 Logic Symbols

Fig. 30-2 Symbol for the AND Gate

One of the basic logic circuits is the AND gate. Its symbol is shown again in figure 30-2. Notice that it has two or more inputs and only one output. The output of an AND gate will be Hi (1) only when *all* the inputs are Hi (1). A Lo (0) signal on *any* of the inputs will cause a Lo (0) on the output. The logic function of an AND gate is to produce a true output only when all the inputs are true. A single false input will produce a false output. This is analogous to the circuit shown in figure 30-3. Obviously all of the switches must be closed for voltage to appear across the Load.

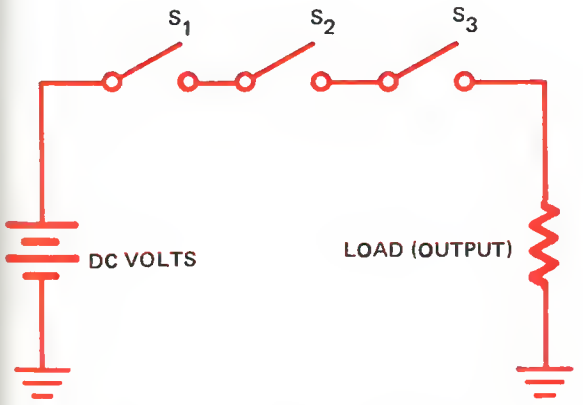


Fig. 30-3 Equivalent Circuit for AND Gate

A second basic logic circuit is the OR gate shown in figure 30-4. This gate also has two or more inputs and one output. The output will be 1 or Hi when any one of the inputs is Hi. The OR gate's logic function is to produce a true (1) output at any time one or more of its inputs is a true. When

Fig. 30-4 Symbol for the OR Gate

none of its inputs are trues (all false), its output will be a false. An important application of OR gates is in the timing of outputs. The gate can be turned on for a period of time by applying a true signal to one of the inputs which will allow the passage of signals. When the true signal is removed, the gate will close. Figure 30-5 shows an electrical equivalent circuit for an OR gate. Closing any one of the switches will produce a voltage across the output.

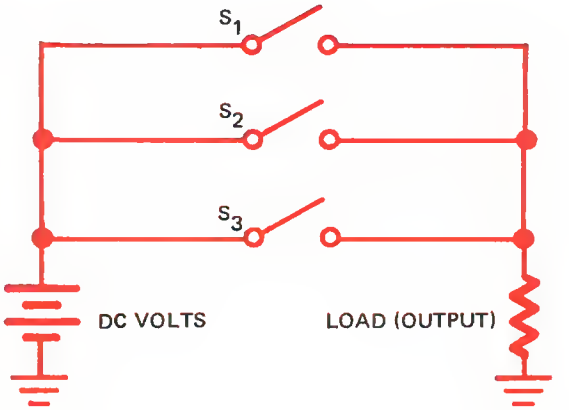
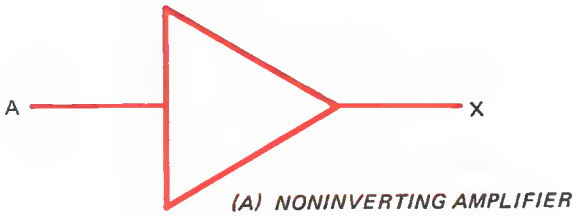


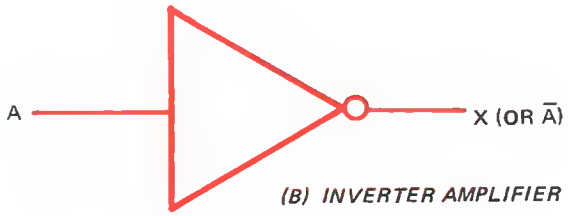
Fig. 30-5 Equivalent circuit for the OR Gate

Amplifiers are extremely important elements in logic circuitry. They are used to build up the signal when it gets too weak to maintain the appropriate logic signal levels. These amplifiers are normally operated in the active region and function as linear pulse amplifiers. They also perform one other important function, that of signal inversion. These inverter amplifiers have one input and



(A) NONINVERTING AMPLIFIER

A	X
Lo	Lo
Hi	Hi



(B) INVERTER AMPLIFIER

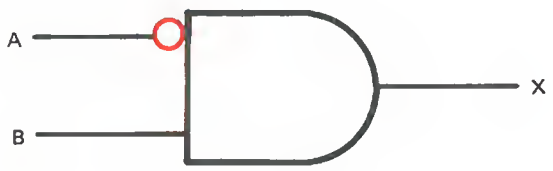
A	X
Lo	Hi
Hi	Lo

Fig. 30-6 Standard and Inverter Amplifiers

one output. The amplifier output is inverted from the input. It is said to be the complement of the input. Figure 30-6 shows the two amplifier symbols.

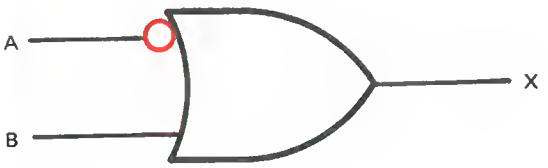
Notice the small circle at the tip of the inverter amplifier. This mark indicates inversion of the signal. It is also used with several other logic symbols and always indicates an inversion. The inversion symbol is often called a Lo-state indicator. This is to say that the Lo-state is the significant state. Conversely, of course, if the symbol is not there, the Hi-state is considered the significant or normal state. The same symbol is often used at the input of logic blocks as shown in figure 30-7. This gate produces a hi output only when a Lo signal occurs at A, while a Hi signal is occuring at B. Another possibility is the OR gate with an inverted input, shown symbolically in figure 30-8. The output of this gate will be Hi if the A input is lo OR if the B input is Hi. The inversion indicator may be used on the inputs of amplifiers, gates and switching elements; in any case it indicates an inversion.

The inversion dot can likewise appear at the output (usually of amplifiers and gates) and means that the output is inverted for normal inputs. The OR gate in figure 30-9



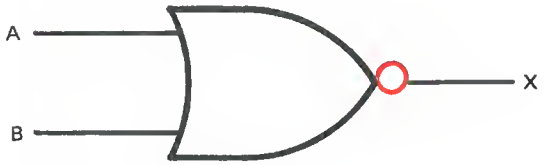
A	B	X
Lo	Lo	Lo
Lo	Hi	Hi
Hi	Lo	Lo
Hi	Hi	Lo

Fig. 30-7 The Inverted Input AND Gate



A	B	X
Lo	Lo	Hi
Lo	Hi	Hi
Hi	Lo	Lo
Hi	Hi	Hi

Fig. 30-8 The Inverted Input OR Gate



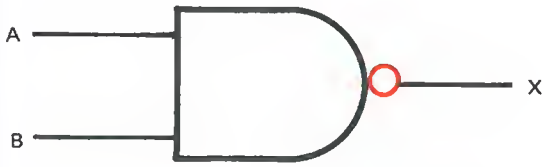
A	B	X
Lo	Lo	Hi
Lo	Hi	Lo
Hi	Lo	Lo
Hi	Hi	Lo

Fig. 30-9 Inverted OR Gate (NOR Gate)

has its output inverted. Inverting the output or an OR gate gives us a NOR gate. This can be accomplished by following a normal OR gate with an inverter amplifier. The logic function of the NOR gate is to produce a Hi at the output only when all the inputs are Lo at one time. If any one of the inputs is Hi, a Lo output will result.

The same sort of situation exists with the inverted AND or NAND circuit. Such a case is shown in figure 30-10. This circuit can be obtained by following an AND gate with an inverter amplifier. This type of gate produces a Lo at the output when all of the inputs are Hi. Another benefit of the NAND gate is to provide level restoration.

The NAND gate is the basic logic circuit and from it all other logic circuits can be



A	B	X
Lo	Lo	Lo
Lo	Hi	Hi
Hi	Lo	Hi
Hi	Hi	Lo

Fig. 30-10 Inverted AND Gate (NAND Gate)

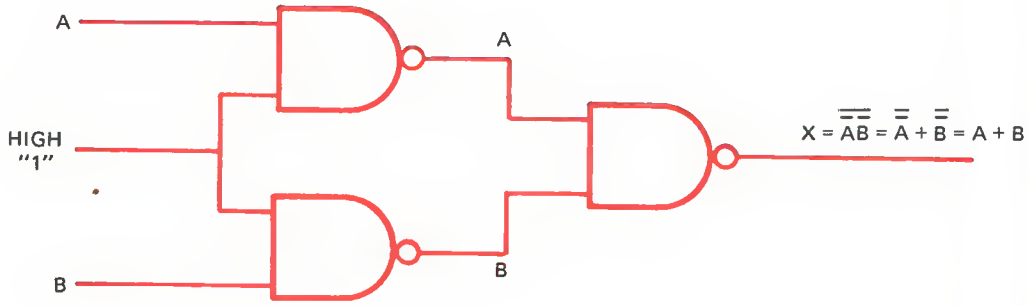


Fig. 30-11 Phantom OR Gate

implemented. For instance, suppose there is an abundance of NAND gates on hand, but an OR gate is needed immediately. As shown in figure 30-11, this problem can be easily solved.

This configuration gives the outputs associated with an OR circuit and is but one of the many examples of NAND gate implementation.

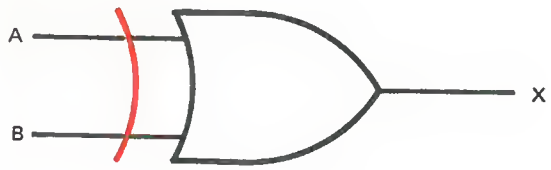


Fig. 30-12 Exclusive OR Gate

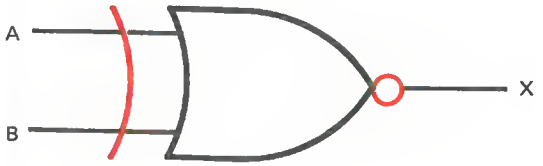
The symbol in figure 30-12 is that of the *Exclusive OR.* The Exclusive OR Gate produces a true output any time the inputs are **not** the same. When the outputs are the same, the output is false. To say this differently, the Exclusive OR produces a **true output if one and only one** of the inputs is false. The truth table for this type of gate is shown in figure 30-13. When A and B are both high, or when both of the inputs are low, the output will be low. However, if either input A or B is low while the other is high, then the output of the gate will be high. These conditions are shown in the truth table.

A	B	X
Lo	Lo	~~Hi~~
Lo	Hi	Hi
Hi	Lo	Hi
Hi	Hi	Lo

Fig. 30-13 Exclusive OR Truth Table

If the Exclusive OR is followed by an inverter, the result will be a compliment of the Exclusive OR gate. This arrangement is shown in figure 30-14. This configuration is sometimes called the coincidence gate. It produces a Hi if all its inputs are Lo or if all the inputs are Hi.

The next basic-logic circuit is the flip-flop. It can have one or more inputs and two outputs. The basic-logic function of a flip-flop is storage. This device remembers what its last impulse was. It remains in one state until triggered to the other state. The storage capability of the flip-flop makes it a very



A	B	X
Lo	Lo	Hi
Lo	Hi	Lo
Hi	Lo	Lo
Hi	Hi	Hi

Fig. 30-14 Inverted Exclusive OR Gate

important unit in digital logic systems. All digital systems are made up by grouping of this basic circuit with gates, amplifiers, and delays.

An interesting approach to producing a flip-flop is to consider it as two NAND gates connected as shown in figure 30-15. Gate A's output is connected to one input of gate B and gate B's output is connected to one A input.

Let's assume an initial starting condition of Q = 1 and $\overline{Q}$ = 0. Starting with inputs of 1 on S and 0 on R at the same time we can see that gate B will have two 1 inputs so $\overline{Q}$ will stay at 0 and gate A will have two 0 inputs so Q will stay at 1.

Now let's put a 0 on S and a 1 on R at the same time. The inputs of Gate B become 0 and 1 (from Q feedback loop) so $\overline{Q}$ goes to 1. Now gate A has two 1 inputs so Q goes to 0. Since Q is feedback to B, this gate will have two 0 inputs and $\overline{Q}$ will be locked at 1. In a similar manner, the inputs of R both become 1 and therefore Q is locked at 0.

Now let's put a 1 on S and a 0 on R. Since $\overline{Q}$ is fed back to gate A, this gate has inputs of 1 and 0 so Q goes to 1 and thus gate B has two 1 inputs so Q goes to 0. Again, due to the feedback loop, A has two 0

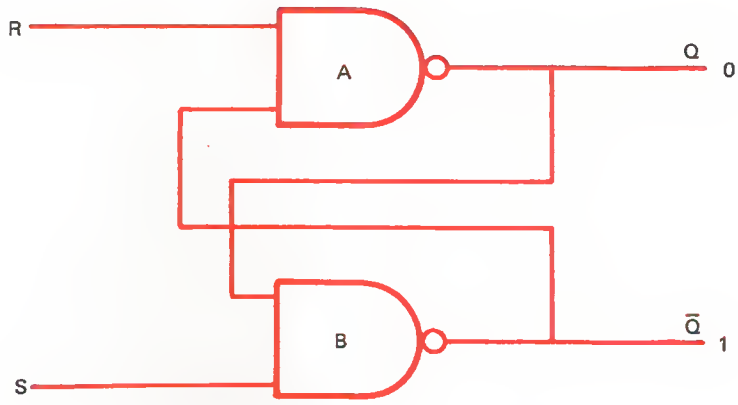


Fig. 30-15 NAND Gate Flip-Flop

inputs so Q is locked at 1 and gate B has two 1 inputs so Q is locked at 0.

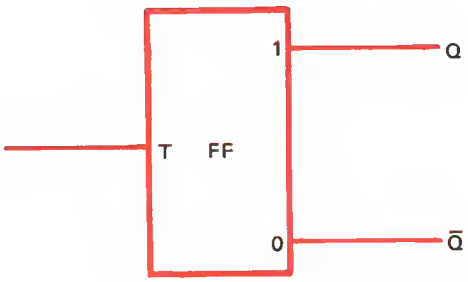
The state of a particular FF is available on an output line (Q) and the FF is identified by what is stored in it. The second output line is usually brought out and labeled $\overline{Q}$ (not Q). This output is the complement (inverse) of the stored function. The inputs of most FFs can receive either level or pulse signals.

Flip-flops may be either clocked or unclocked. Clocking is the practice of feeding pulses of a given PRF to the flip-flop gates so that the gates will be open and closed at particular instances of time. Clocked flip-flop outputs will respond to the inputs only at the proper clock times. The output of the unclocked FF will respond anytime the inputs change.

Figure 30-16 shows the symbol for the toggle flip-flop. It is a bistable with one input line and two outputs. The outputs change state from one input pulse to the next. It is stable in either state and remains in that state until another pulse is applied. Since this is the case, the state after a trigger pulse cannot be predicted unless the previous state is known.

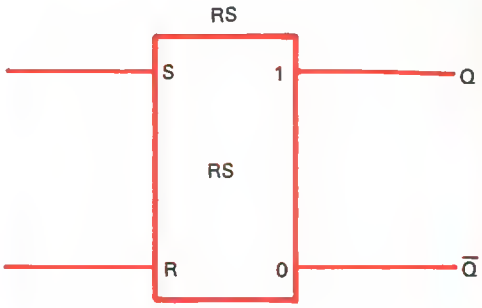
The set reset flip-flop (RS FF) is a bistable with two input lines and two output lines. The outputs are opposite and respond with state changes when the inputs change. RS FFs are always *set to 1* and *reset to zero*. An input signal is used at the S terminal to switch the device to a known Hi state. The device is reset to zero by a signal on the reset line and places the FF in the Lo state. Inputs to the S and R terminals must not be applied simultaneously because the device can be in only one state at a time. Therefore, use of the RS FF is limited to applications where both inputs will not be activated at the same time. Figure 30-17 shows the symbol and truth table for a typical RS FF.

Since the RS FF has an uncertain state, a need arises for another type. The J-K flip-flop has no such uncertain state. Figure 30-18 shows the symbol for a J-K FF. This unit has two inputs and two outputs. A Hi input at J switches the FF to the Hi state. If Hi's are applied to K, the FF switches to Lo. If J and K receive Hi's at the same time, the FF switches to the compliment (if it was Hi, it goes Lo and vice versa). Applying Lo's to both inputs produces no change. The J is the set line and K is the reset line. The J-K flip-flop is much more than a simple



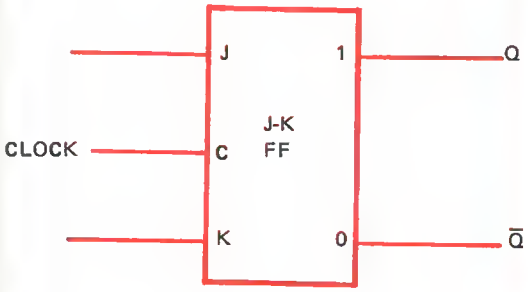
INPUT		OUTPUT	
Before Trigger Pulse		After Trigger Pulse	
Q	$\overline{Q}$	Q	$\overline{Q}$
Lo	Hi	Hi	Lo
Hi	Lo	Lo	Hi

Fig. 30-16 Symbol for Toggle FF



INPUT		OUTPUT	
R	S	Q	$\overline{Q}$
Lo	Lo	Will Not Change	
Lo	Hi	Hi	Lo
Hi	Lo	Lo	Hi
Hi	Hi		

Fig. 30-17 Symbol for an RS FF



INPUT		OUTPUT	
J	K	Q	$\overline{Q}$
Lo	Lo	No Change	
Lo	Hi	Lo	Hi
Hi	Lo	Hi	Lo
Hi	Hi	Compliment	

Fig. 30-18 Symbol for the J-K FF

flip-flop (TFF); it normally is either a dual rank or AC-coupled flip-flop. The AC coupling method uses the RC time constant of the capacitive input for short term storage of the input information. The dual rank method is faster than the slow capacitor discharge. It actually combines two flip-flops, one for input storage and one for output storage. Several gates are also used in it to form a single logic element. All of this is not usually indicated by the logic symbol.

The actual operation of the J-K (either type) is the action of the two FFs and the clock pulse at the gates. With a Hi input at J, only the leading edge of the clock pulse stores the input information at J. The trailing edge sets the FF. With a Hi input at K, only the leading edge of the clock pulse stores the input information at K, and the trailing edge of the clock pulse stores the input information at K. The trailing edge of the clock pulse also resets the FF. When both J and K have Hi inputs, the leading edge of the clock pulse stores information at both J and K. The trailing edge of the clock pulse switches the state of the FF.

There are several other major types of flip-flops. You may wish to review the operation of these others on your own. They will not be discussed here.

MATERIALS

2 DC power supplies
1 Lab oscilloscope or VOM
3 IC, type SN15830N dual 4-input NAND/NOR gate, or equivalent, and data sheet
4 IC sockets

PROCEDURE

1. The TI SN15830N is dual 4-input NAND/NOR gate. Prepare the IC for observation. Obtain the correct supply voltage from the data sheet.

2. Since this IC has 4 inputs tie them together so that there will be only 2 inputs as shown in figure 30-19.

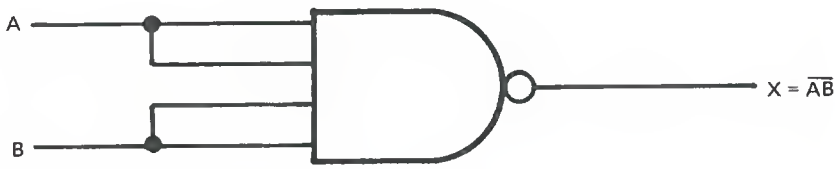


Fig. 30-19 Pairing Inputs to NAND Gate

3. Obtain the output for all 4 possible combinations of inputs A and B. Record these values in an appropriate truth table form.

4. Now construct the NOT (INVERTER) circuit as shown in figure 30-20 and repeat step 3.

Fig. 30-20 Construction of NOT Circuit for NAND Gate

5. Now construct the AND circuit shown in figure 30-21 and repeat step 3.

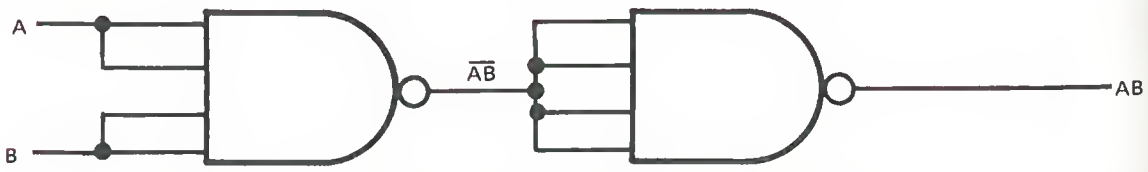


Fig. 30-21 Construction of AND Circuit from NAND Gates

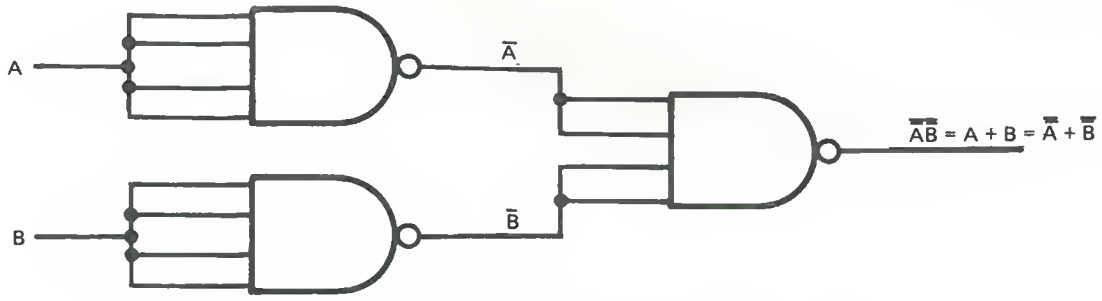


Fig. 30-22 Construction of OR Circuit from NAND Gates

6. Now construct the OR circuit shown in figure 30-22 and repeat step 3.
7. Now construct the NOR circuit shown in figure 30-23 and repeat step 3.

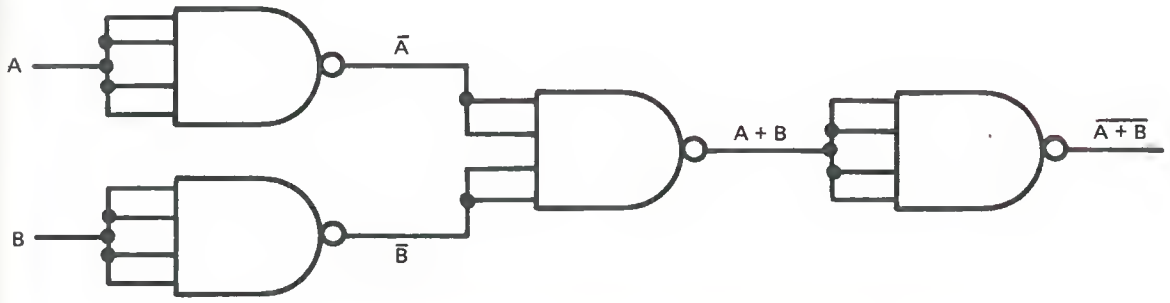


Fig. 30-23 Construction of NOR Circuit from NAND Gate

8. Construct the EXCLUSIVE-OR circuit as shown in figure 30-24 and repeat step 3.

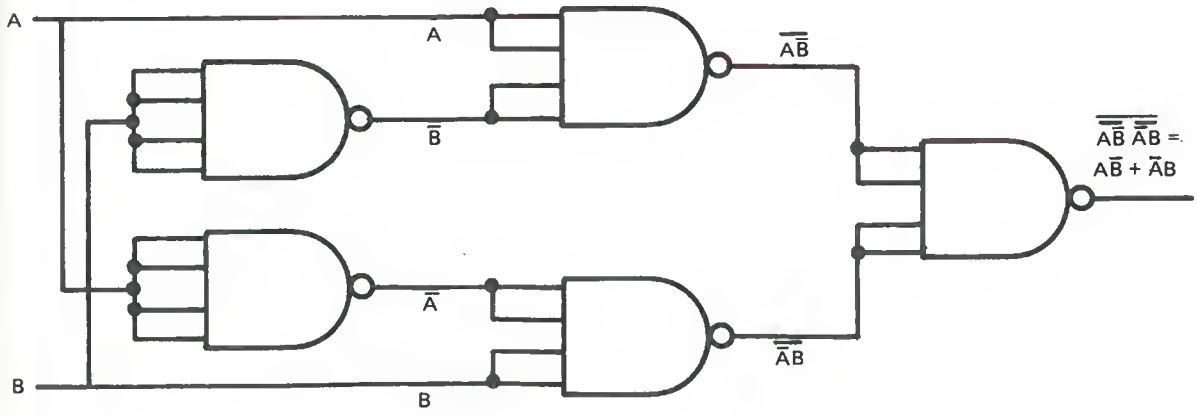


Fig. 30-24 Construction of EXCLUSIVE-OR Circuit from NAND Gates

9. Construct the COINCIDENCE circuit as shown in figure 30-25 and repeat step 3.

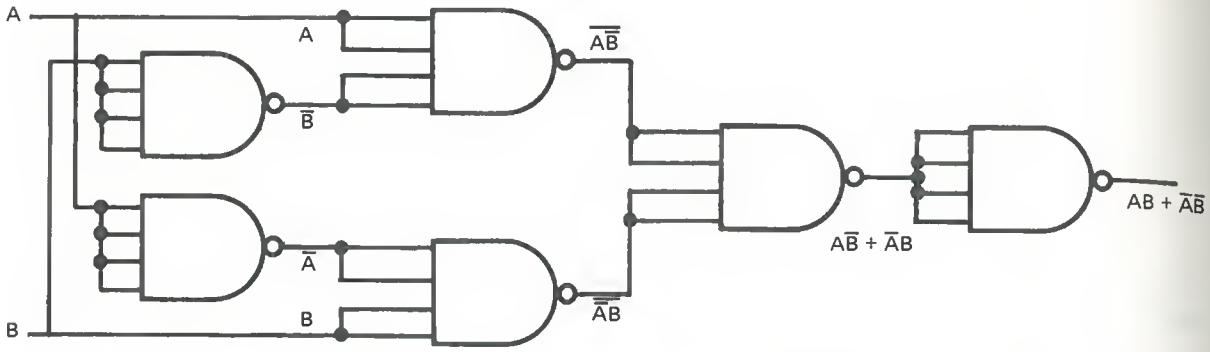


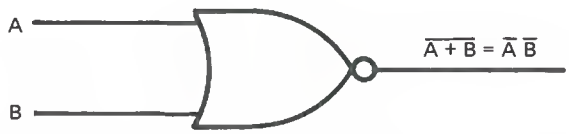
Fig. 30-25 Construction of COINCIDENCE Circuit from NAND Gates

10. Construct the RS flip-flop circuit as shown in figure 30-15 and obtain and record data in truth table form to describe the operation of the flip-flop. The triggering circuit of experiment 19 should be connected such that when a 1 is applied to one of the inputs, a 0 will be applied to the other.

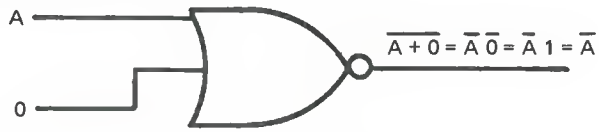
ANALYSIS GUIDE. In analyzing the results of this experiment you should describe the basic logic devices and how they work to achieve their logical purposes.

PROBLEMS

1. Convert the decimal number 225.672 to binary.
2. It was stated in the discussion that the NAND gate is the basic logic gate and from this all others can be implemented. There is one other gate which is perhaps just as basic and can also be used to implement all other gates. This is the NOR gate shown below.



We can see that if we want the output of this device to be only $\overline{A}$, then $\overline{B}$ must be equal to 1 so that the Boolean identity $\overline{A}1 = \overline{A}$ can pertain. Therefore, if $\overline{B} = 1$ then $B = 0$. So by tieing all except one of the inputs of the NOR gate to 0 we can implement a NOT gate as shown below.



Now using only NOR gates implement an AND circuit, an OR circuit, and a NAND circuit. Be sure to label the inputs to *each* NOR gate included in these circuits.

EXPERIMENT 1 _____ Name _____

Date: _____ Class _____ Instructor _____

Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary
1		26		51		76	
2		27		52		77	
3		28		53		78	
4		29		54		79	
5		30		55		80	
6		31		56		81	
7		32		57		82	
8		33		58		83	
9		34		59		84	
10		35		60		85	
11		36		61		86	
12		37		62		87	
13		38		63		88	
14		39		64		89	
15		40		65		90	
16		41		66		91	
17		42		67		92	
18		43		68		93	
19		44		69		94	
20		45		70		95	
21		46		71		96	
22		47		72		97	
23		48		73		98	
24		49		74		99	
25		50		75		100	

(A)

Binary	Decimal
111011101	
11101101	
10110.1101	
.11011	
.10001	

(B)

Decimal	Binary
353	
557	
632	
0.725	
0.5625	

(C)

Fig. 1-3 The Data Tables

Binary	Decimal
4.(a)	
4.(b)	
4.(c)	
5.(a)	
5.(b)	

(D)

Binary	Decimal
6.	
7.	

(E)

Fig. 1-3 The Data Tables (Cont.)

EXPERIMENT 2 _____ Name _____

Date: _____ Class _____ Instructor _____

THEOREM 3(b)		A X 0 = 0
	A	A X 0 = 0
	1	X =
	0	X =

THEOREM 6(b)				(A X B) + (A X C) = A X (B + C)
	A	B	C	(A X B) + (A X C) = A X (B + C)
				X + X = X + =
				X + X = X + =
				X + X = X + =
				X + X = X + =
				X + X = X + =
				X + X = X + =
				X + X = X + =
				X + X = X + =

TRUTH TABLE FOR Fig. 2-10		BOOLEAN EXPRESSION Fig. 2-10
A	B	
0	0	
0	1	
1	0	
1	1	

Fig. 2-10 SIMPLIFIED EXPRESSION		Simplified Circuit
A	B	

Fig. 2-12 The Data Tables

Fig. 2-11 BOOLEAN EQUATION			
A	B	C	

SIMPLIFIED EQUATION Fig. 2-11			

THEOREM 8	
BOOLEAN EXPRESSION	
A	
1	
0	

Fig. 2-12 The Data Tables (Cont.)

EXPERIMENT 3 Name _____

Date: _____ Class _____ Instructor _____

DC Volts	10	11	12	13	14	15
Power Supply Reading (Multimeter)						
Oscilloscope Reading						

Audio Generator Hz	30	60	100	200	500	1000
Time Duration 1/2 Cycle						
Frequency						

AC Volts	1	2	3	4	5
Multimeter Reading					
Oscilloscope Reading					

Frequency	100 Hz	500 Hz	1 kHz
Rise Time			

Fig. 3-5 The Data Tables

EXPERIMENT 4 Name _____

Date: _____ Class _____ Instructor _____

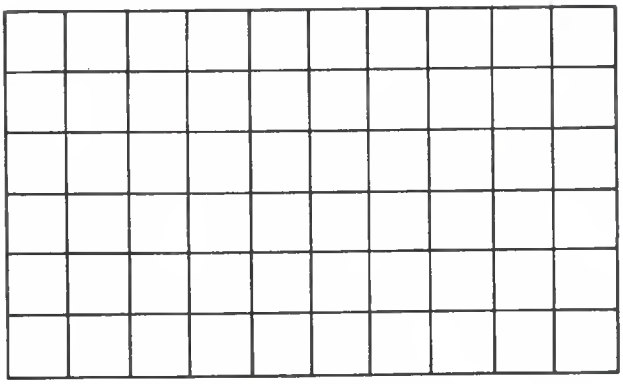
Waveform	Period Set	Freq Set	Period Read	Freq Read	T_d	% DC	T_R	T_F	Identity of Wave
50% DC									
0.1 μF CAP Parallel									
Inductor Parallel									
10 KC Pulse T_d = 10 μsec									

Sketch of First Waveform

Sketch of Second Waveform

Fig. 4-11 The Data Tables

Sketch of
Third Waveform



Sketch of
Fourth Waveform

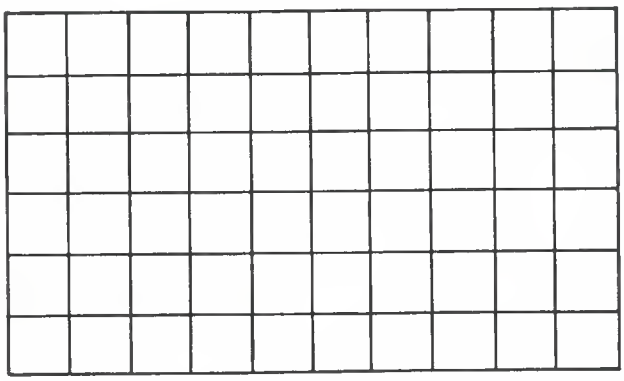


Fig. 4-11 The Data Tables (Cont'd)

EXPERIMENT 5 Name _____

Date: _____ Class _____ Instructor _____

I_B μA	0	40	60	80	100	120	140
V_{CE} volts	I_C	I_C	I_C	I_C	I_C	I_C	I_C
0							
2							
4							
6							
8							
10							
12							
14							
16							
18							
20							

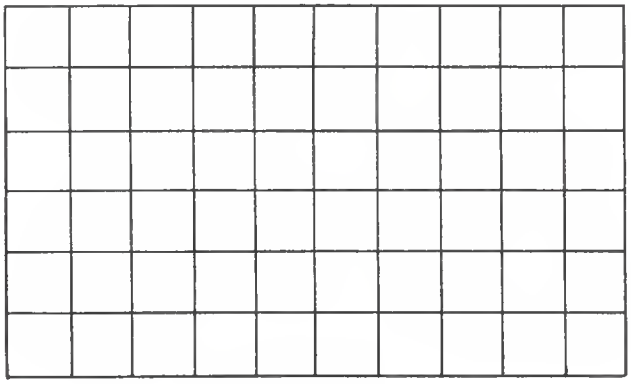
V_{CE} =	-1.0V	-5.0V	-10.0V	-20.0V
I_B μa	V_{BE}	V_{BE}	V_{BE}	V_{BE}
0				
10				
20				
30				
40				
60				
80				
120				
160				

Fig. 5-17 The Data Tables

EXPERIMENT 6 Name _____

Date: _____ Class _____ Instructor _____

CALCULATIONS R_L



Waveform

R_B CALCULATIONS

Fig. 6-10 The Data Tables

	DELAY TIME	RISE TIME	PULSE DURATION	STORAGE TIME	FALL TIME
FIRST CKT					
OUTPUT R_B					
POINT X R_B					
OUTPUT R_BC_B					
POINT X R_BC_B					
OUTPUT (Three Steps Above C_B)					
POINT X (Three Steps Above C_B)					
OUTPUT (Three Steps Below C_B)					
POINT X (Three Steps Below C)					

Output Waveform with R_B in the circuit

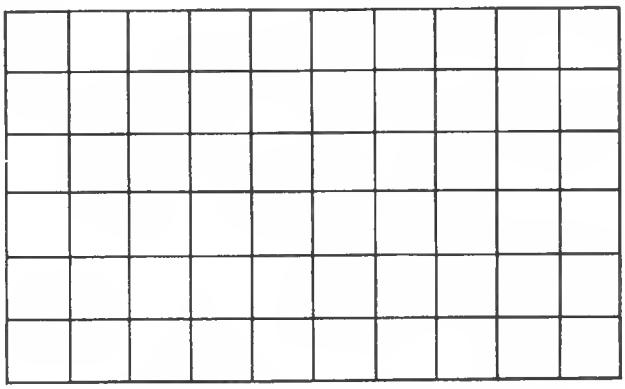
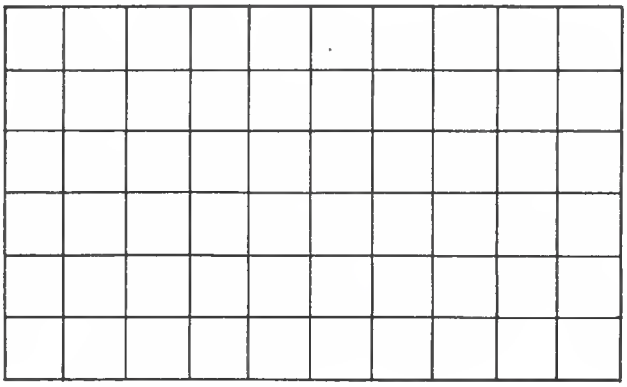


Fig. 6-10 The Data Tables (Cont.)

EXPERIMENT 6 Name _____

Date: _____ Class _____ Instructor _____

Waveform at Point X with R_B in the Circuit



C_B CALCULATIONS

Output Waveform with C_B in the Circuit

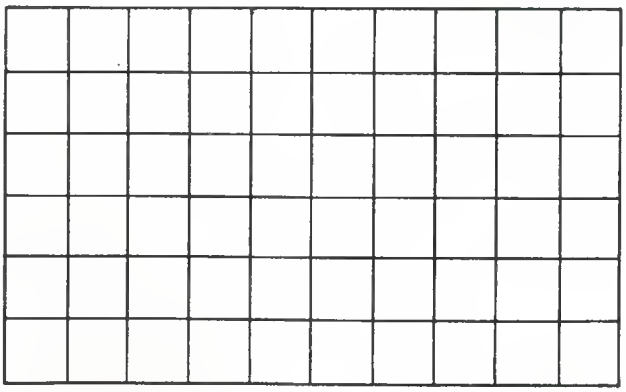
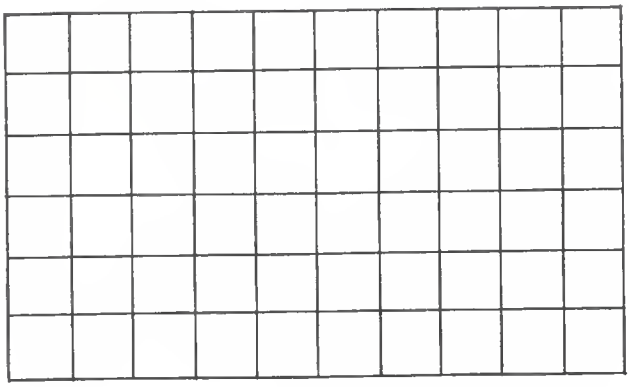
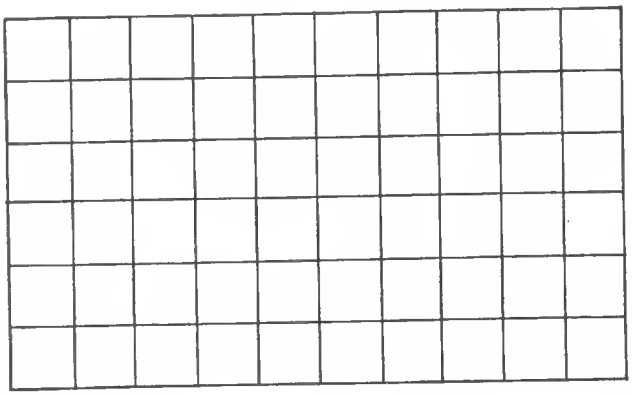


Fig. 6-10 The Data Tables (Cont.)

Waveform at Point X with C_B in the Circuit



Output Waveform with C Three Steps Above C_B



Waveform at Point X with C Three Steps Above C_B

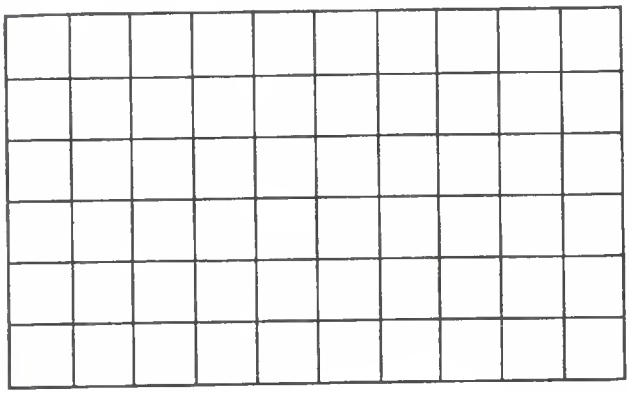
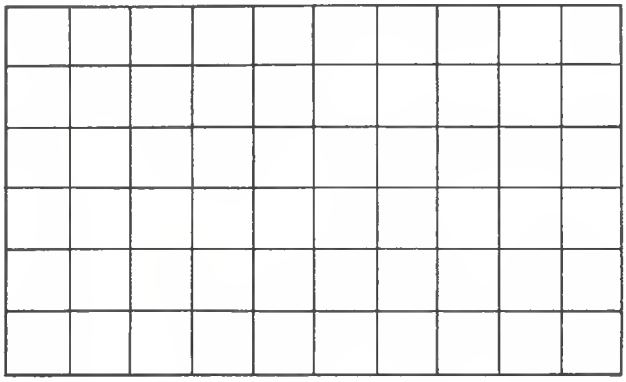


Fig. 6-10 The Data Tables (Cont.)

EXPERIMENT 6 Name _____

Date: _____ Class _____ Instructor _____

Output Waveform With C Three Steps Below C_B



Waveform at Point X With C Three Steps Below C_B

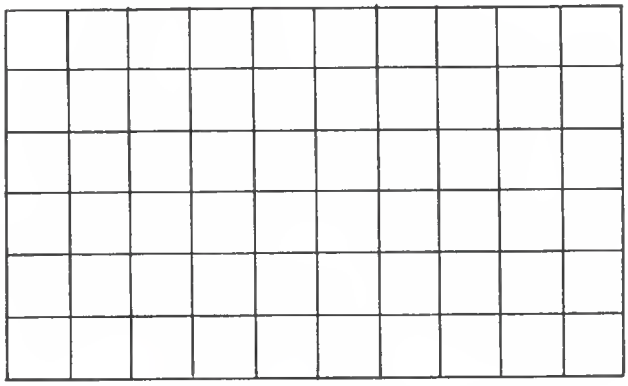


Fig. 6-10 The Data Tables (Cont'd)

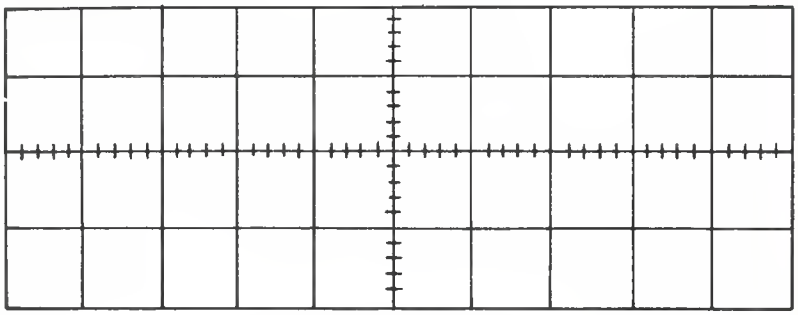
EXPERIMENT 7 Name _____

Date: _____ Class _____ Instructor _____

First Circuit

Amplitude = _____

Period = _____

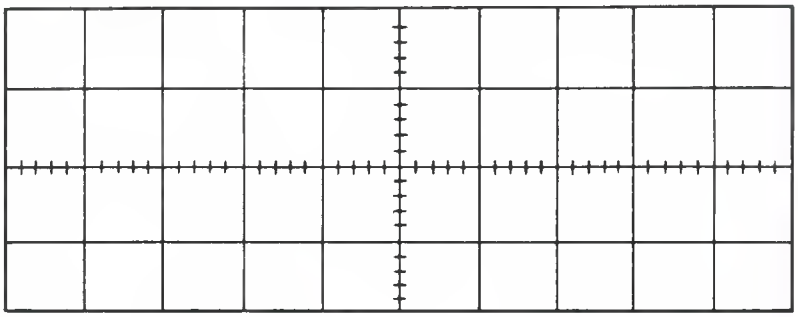


Output Waveform
(Show zero reference level)

Second Circuit

Amplitude = _____

Period = _____

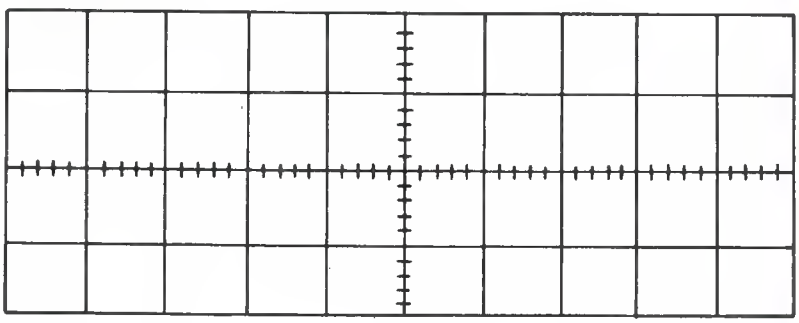


Output Waveform
(Show zero reference level)

Third Circuit

Amplitude = _____

Period = _____



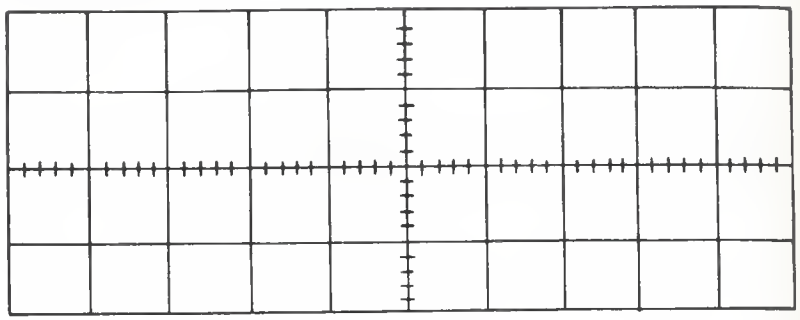
Output Waveform
(Show zero reference level)

Fig. 7-12 The Data Tables

Fourth Circuit

Amplitude = _____

Period = _____



Output Waveform
(Show zero reference level)

Fig. 7-12 The Data Tables (Cont'd)

EXPERIMENT 8 Name _____

Date: _____ Class _____ Instructor _____

	R_B	R_L	V_{CC}	I_B	E_{in}	tLE	tTE
Calculated							
Measure							

Output Resistor Clipper

	R_L	R_2	R_1	V_{CC}	V_{C1}	E_{in}
Calculated						
Measure						

Output Diode Emitter Clamp

Fig. 8-9 The Data Tables

EXPERIMENT 9 Name _____

Date: _____ Class _____ Instructor _____

Input	Output
A = +5	
B = 0	

Output Waveform

Input	Output
A = 0	
B = +5	

Output Waveform

Fig. 9-11 The Data Tables

Input	Output
A = +5	
B = +5	
Circuit Type	

Output Waveform

Input	Output
A = +5	
B = 0	

Output Waveform

Input	Output
A = 0	
B = +3	

Output Waveform

Fig. 9-11 The Data Tables (Cont.)

EXPERIMENT 9 Name _____

Date: _____ Class _____ Instructor _____

Input	Output										
A = +3											
B = +3											
Circuit Type											

Output Waveform

Circuit Diagram for Two Input and Gate

Fig. 9-11 The Data Tables (Cont.)

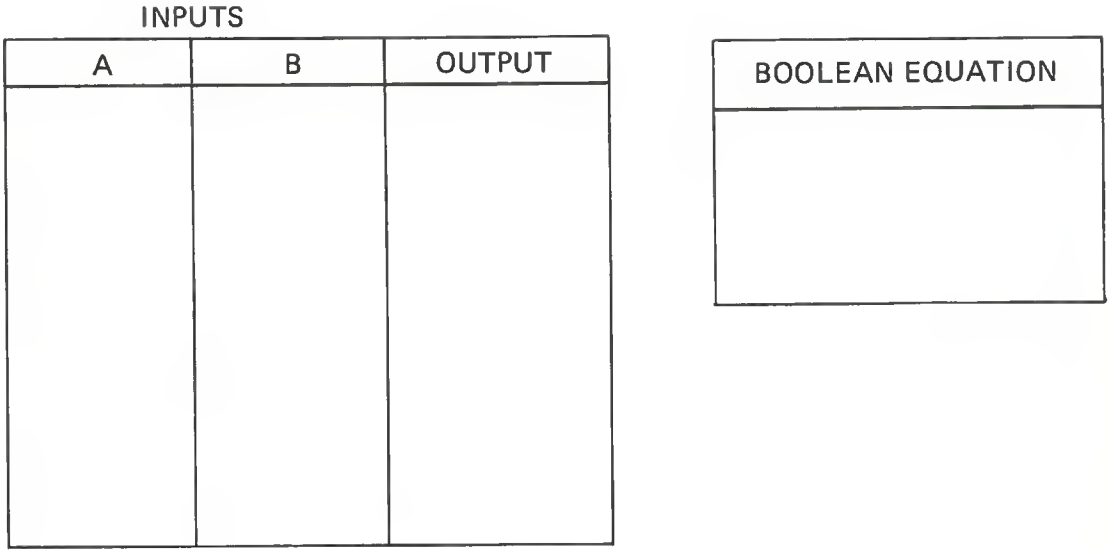


Fig. 9-11 The Data Tables (Cont.)

EXPERIMENT 10 _____ Name _____

Date: _____ Class _____ Instructor _____

	V_{CE} No Input	V_{CE} Input A Only	V_{CE} Input B Only	V_{CE} Input A & B
First Circuit				
Second Circuit				
Third Circuit				
Fourth Circuit				

Measured Data

Fig. 10-9 The Data Table

Circuit Diagram

Fig. 10-9 The Data Table (Cont.)

EXPERIMENT 11

Name _____

Date: _____ Class _____ Instructor _____

First Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts
Boolean Expression				

Second Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts
Boolean Expression				

Fig. 11-7 The Data Tables

Third Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Boolean Expression

Fourth Circuit Data

Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

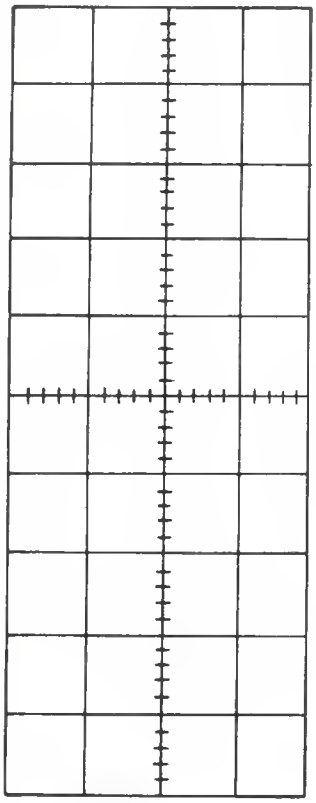
Boolean Expression

Fig. 11-7 The Data Table (Cont'd)

EXPERIMENT 12

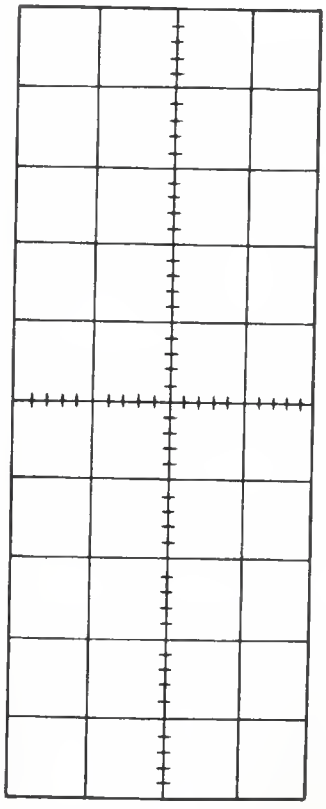
Name _____

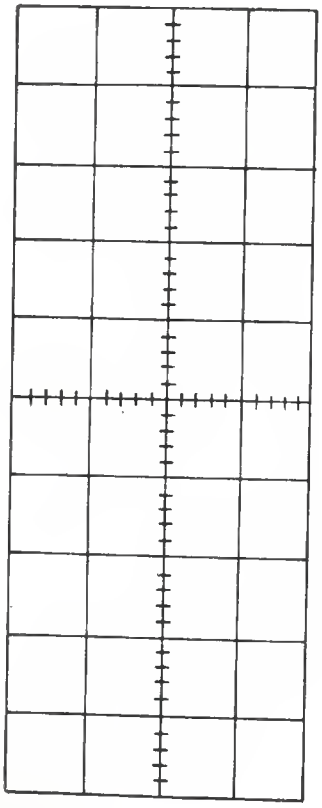
Date: _____ Class _____ Instructor _____



Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Show step numbers and output waveforms. Give all relevant data such as amplitude, period and reference level for each waveform.





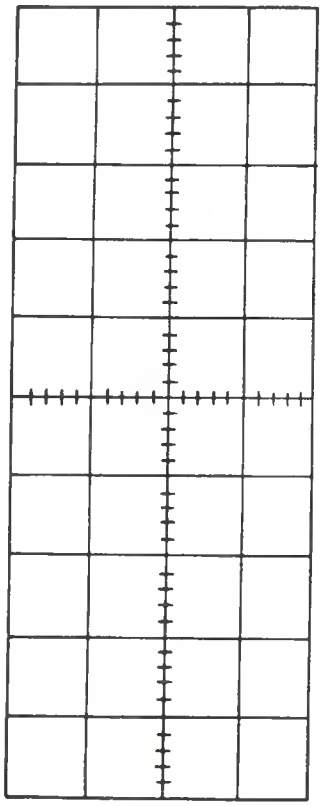
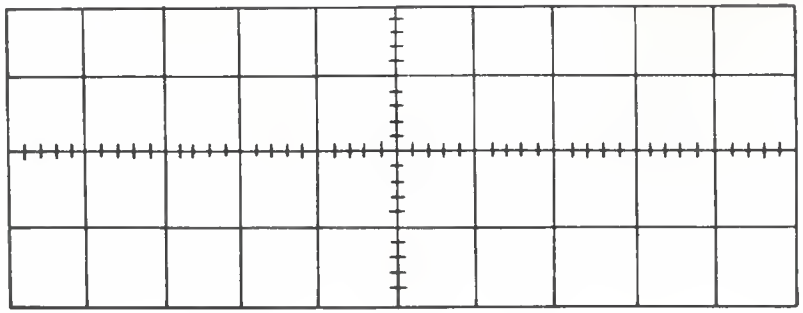
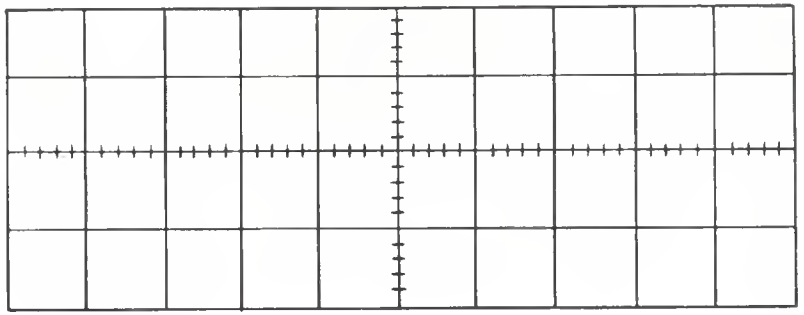
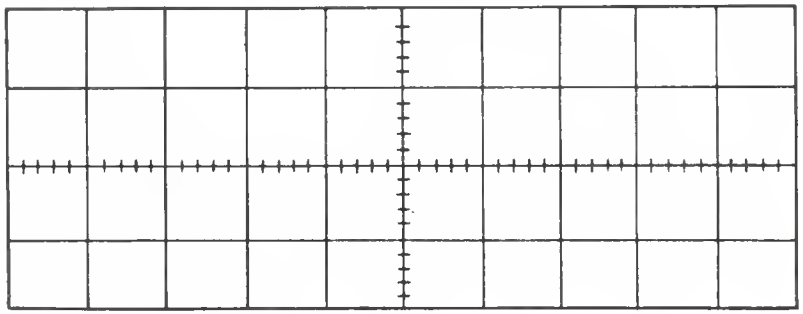
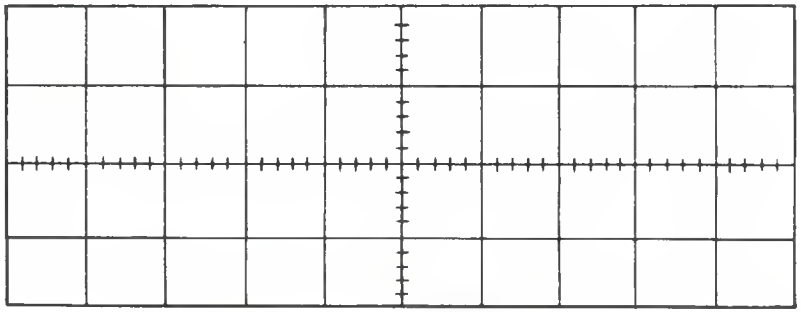


Fig. 12-9 The Data Tables









Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

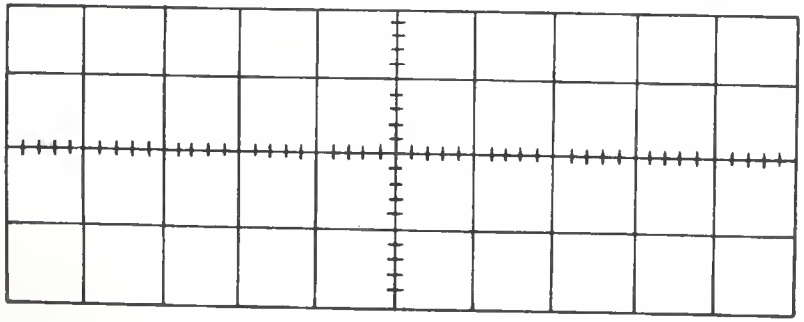
Show step numbers and output waveforms.
Give all relevant data such as amplitude,
period and reference level for each waveform.

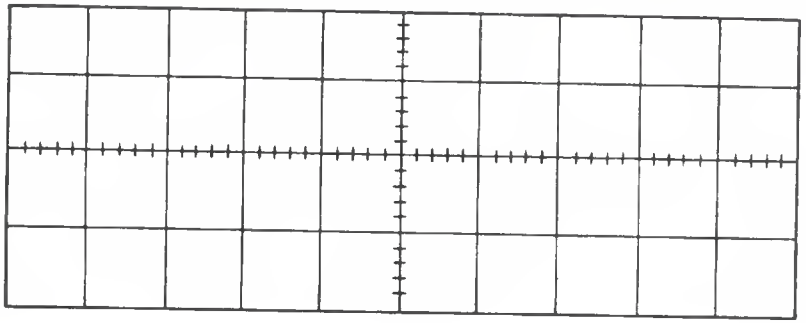
Fig. 12-9 The Data Tables (Cont'd)

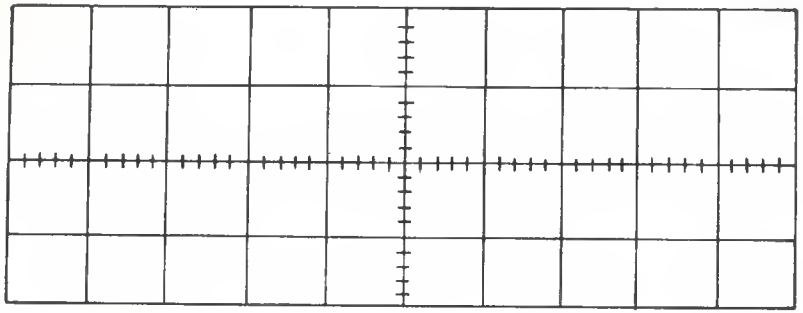
EXPERIMENT 12

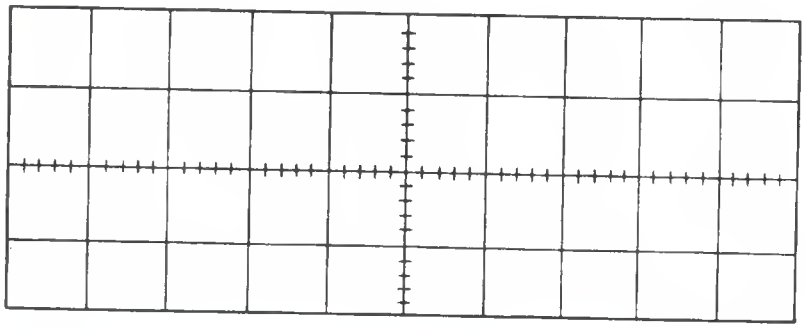
Date: _____ Name _____

Class _____ Instructor _____









Inputs 0 or 1			Output	
A	B	C	0 or 1	volts

Show step numbers and output waveforms. Give all relevant data such as amplitude, period and reference level for each waveform.

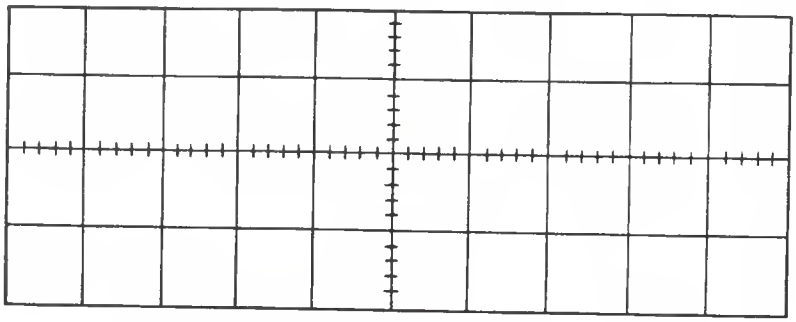
Fig. 12-9 The Data Tables (Cont'd)

EXPERIMENT 13

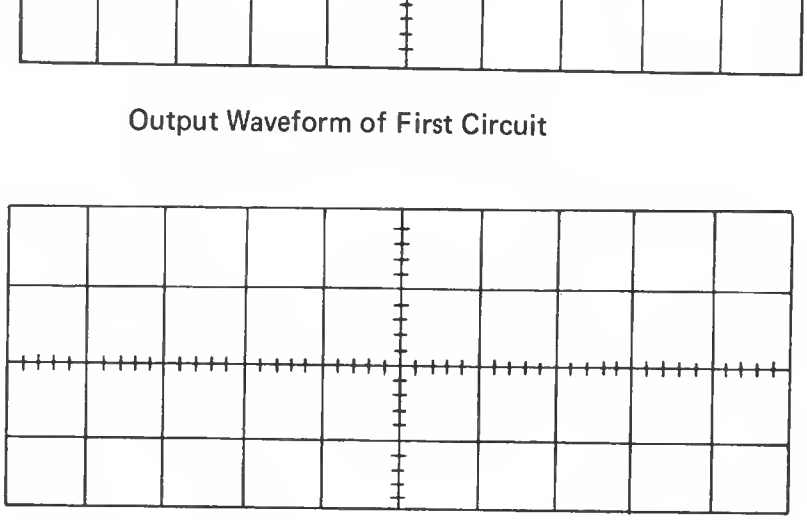
Name _____

Date: _____ Class _____ Instructor _____

f _____



Output Waveform of First Circuit



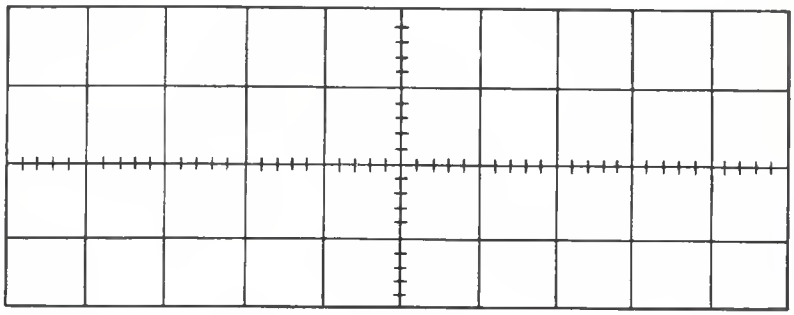
Output Waveform of Second Circuit

EXPERIMENT 14 Name _____

Date: _____ Class _____ Instructor _____

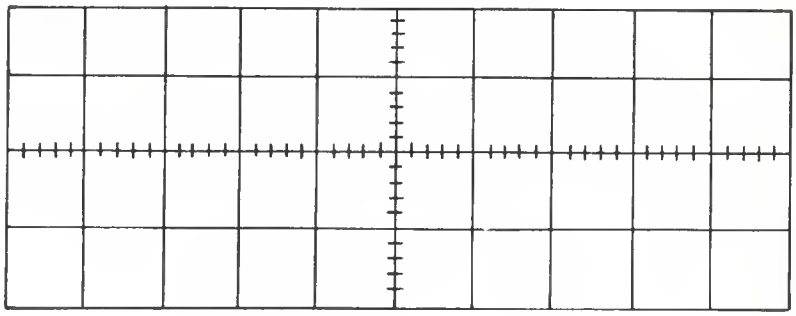
V_{C1} = _____

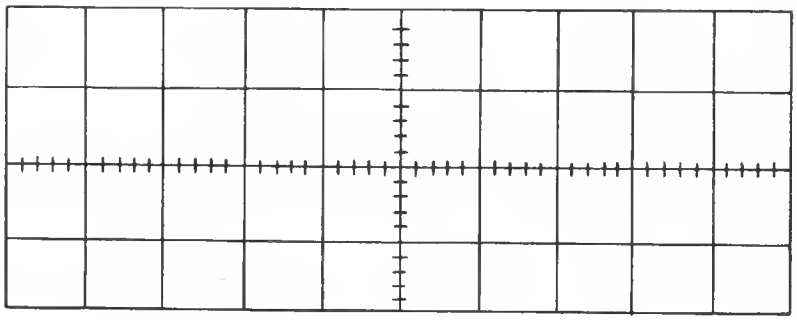
V_{C2} = _____



V_{C1}' = _____

V_{C2}' = _____





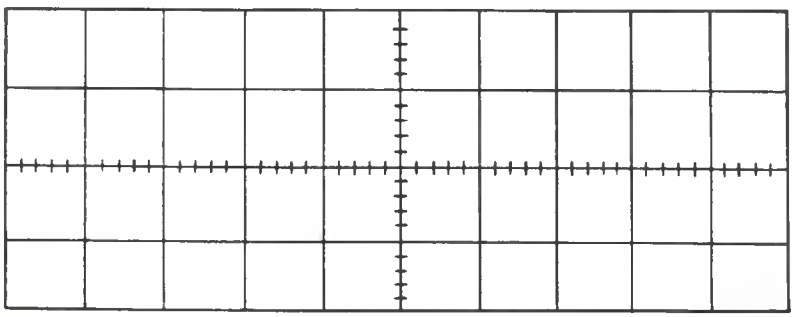
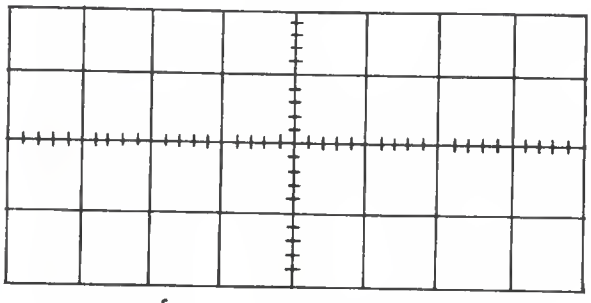


Fig. 14-4 The Data Table

EXPERIMENT 15 Name _____

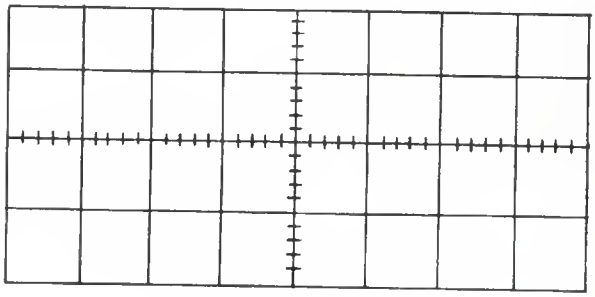
Date: _____ Class _____ Instructor _____

Input



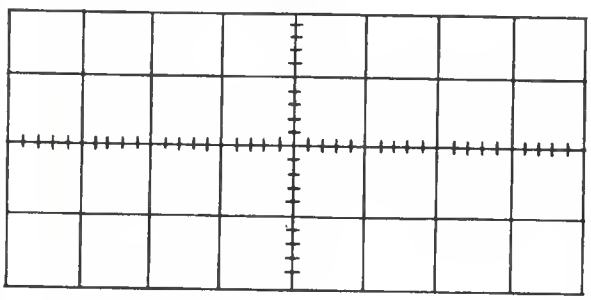
f = _____

Output



f = _____

Output



Output

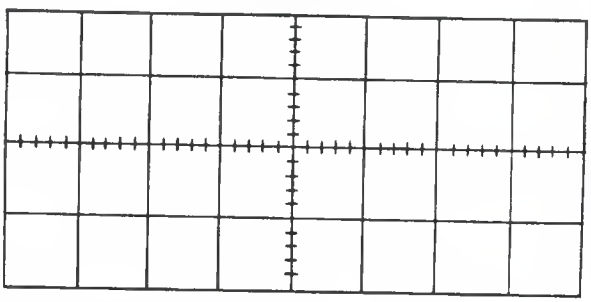


Fig. 15-5 The Data Tables

EXPERIMENT 16 _____ Name _____

Date: _____ Class _____ Instructor _____

R-S Mode Truth Table

t_n				$t_n + 1$	
Inputs				Outputs	
S_1	S_2	C_1	C_2	Q	$\overline{Q}$
0	X	0	X		
0	X	1	X		
1	X	0	X		
X	0	X	0		
X	0	X	1		
X	1	X	0		
0	0	1	1		
1	1	0	0		
1	1	1	1	Indeterminate	

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

X = no input, terminal left floating

J-K Mode Truth Table

t_n		$t_n + 1$
Inputs		Outputs
S_1	C_1	Q
0	0	
0	1	
1	0	
1	1	
X	X	

Triggering Circuit Data

Inputs		Outputs	
S_1	C_1	Q	$\overline{Q}$
X			
	X		
X			
	X		

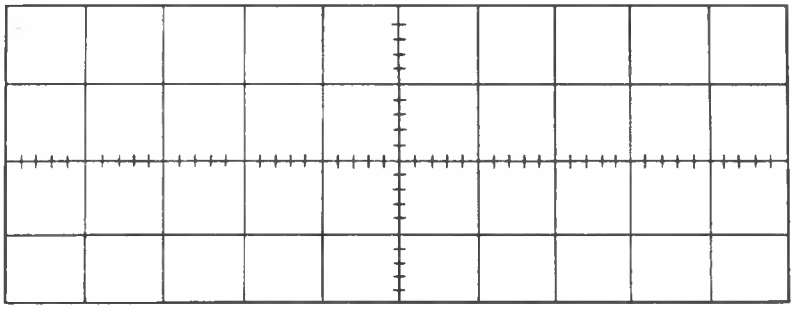
Fig. 16-7 The Data Tables

EXPERIMENT 17 _____ Name _____

Date: _____ Class _____ Instructor _____

R_1 = _____

C_1 = _____



Common Emitter V_{BE}

Effects of varying

R_1 _____

_____

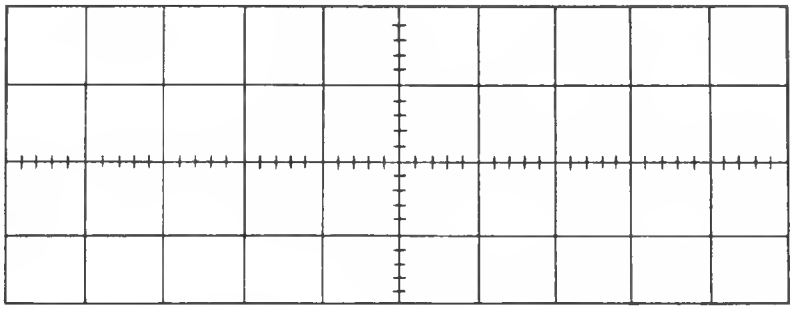
_____

Effects of varying

C_1 _____

_____

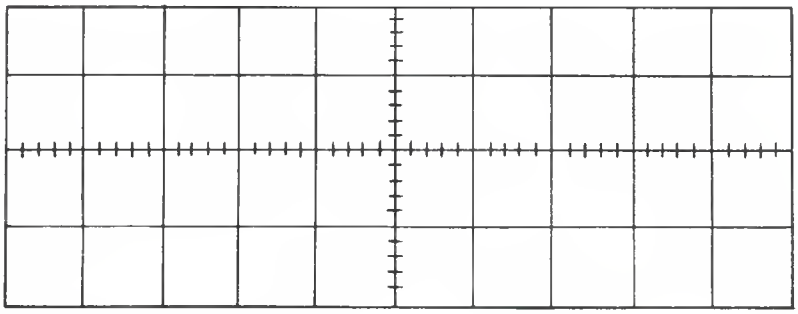
_____



Common Emitter V_{CE}

R_1' _____

C_1' _____



Common Emitter V_{CB}

Effect of varying trigger frequency _____

_____

Effect of varying trigger amplitude _____

_____

Fig. 17-8 The Data Tables

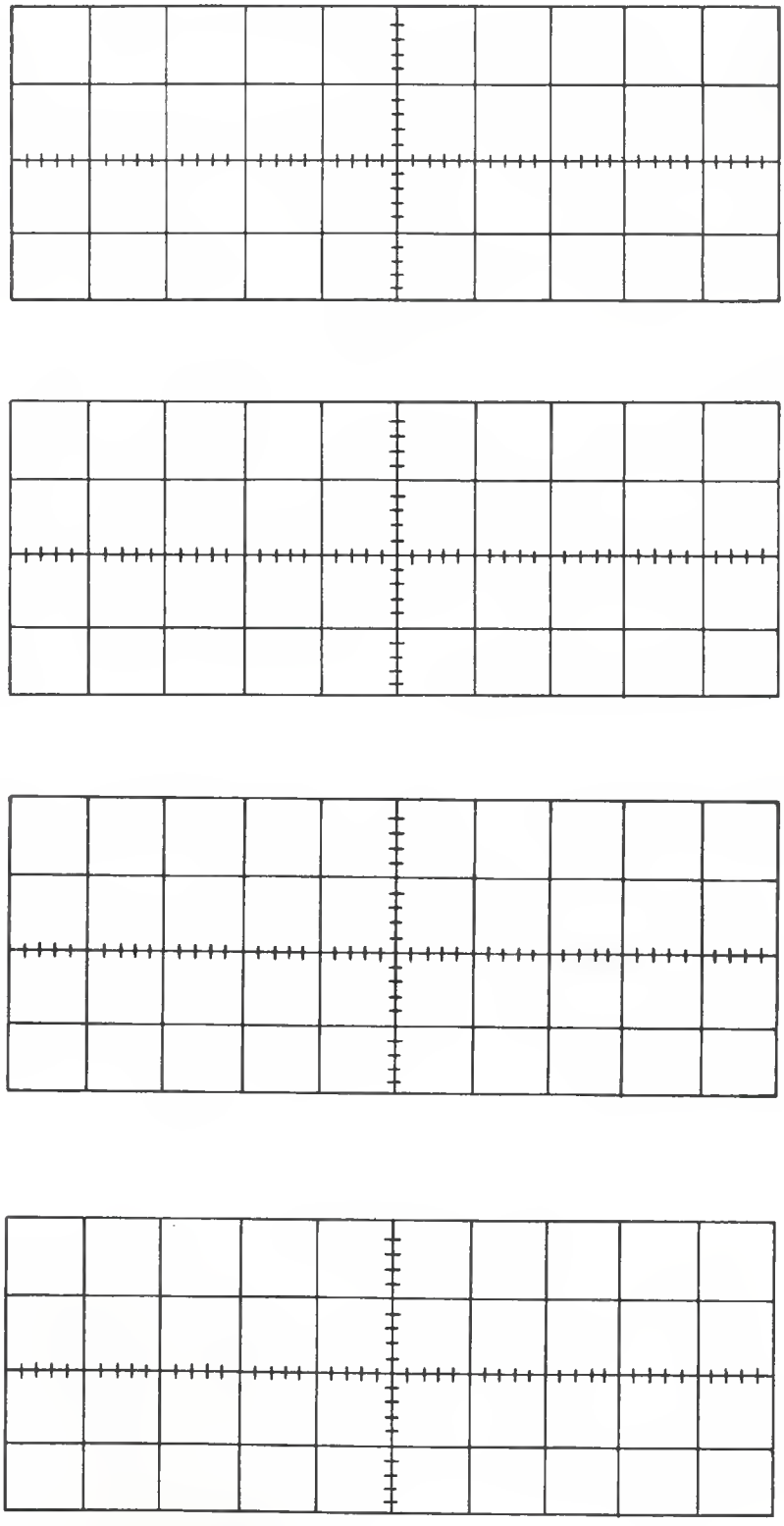
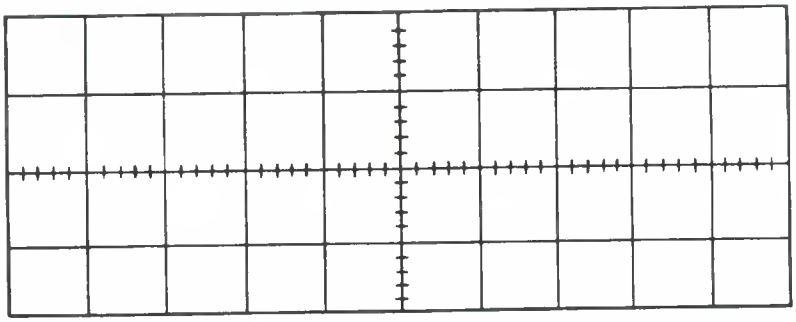
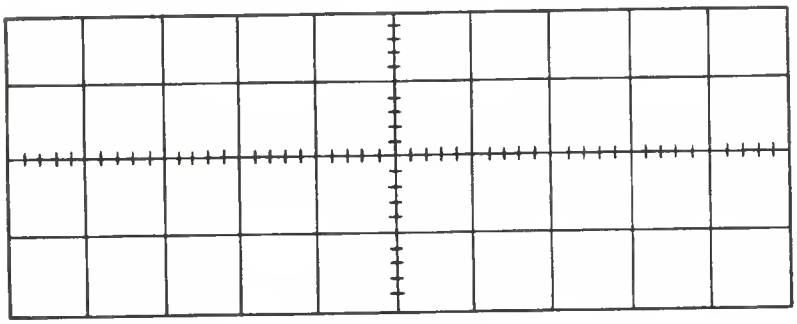
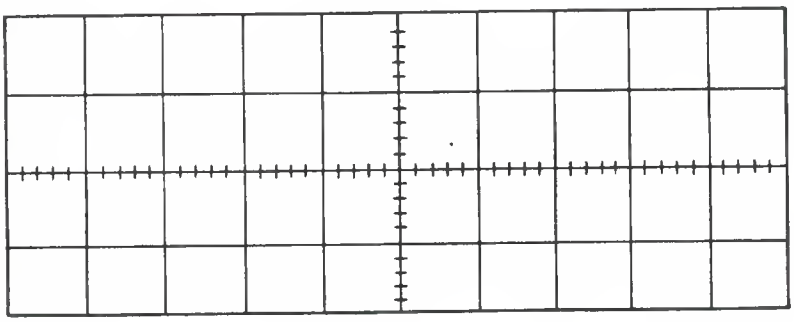


Fig. 18-6 The Results







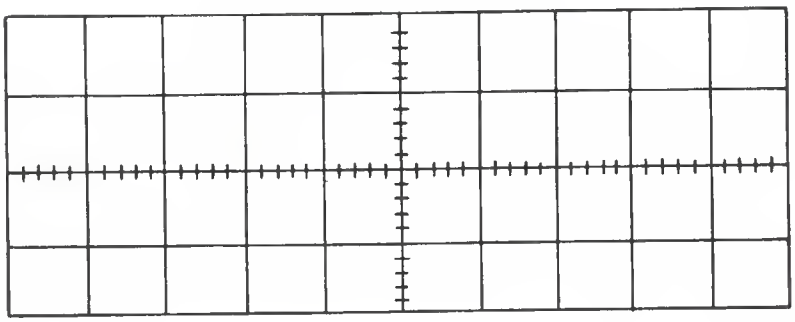


Fig. 18-6 The Results (Cont'd)

EXPERIMENT 19 _____ Name _____

Date: _____ Class _____ Instructor _____

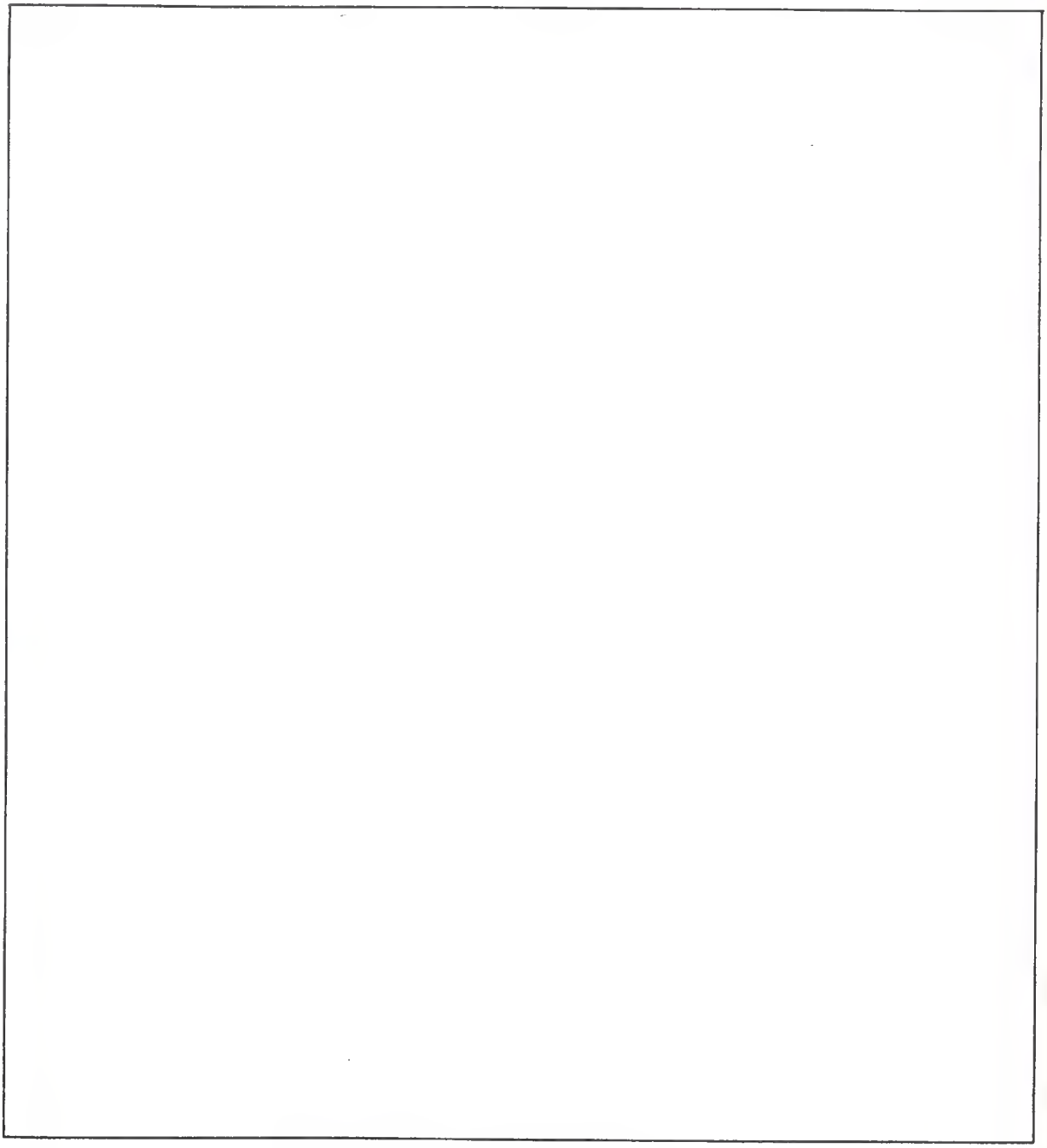
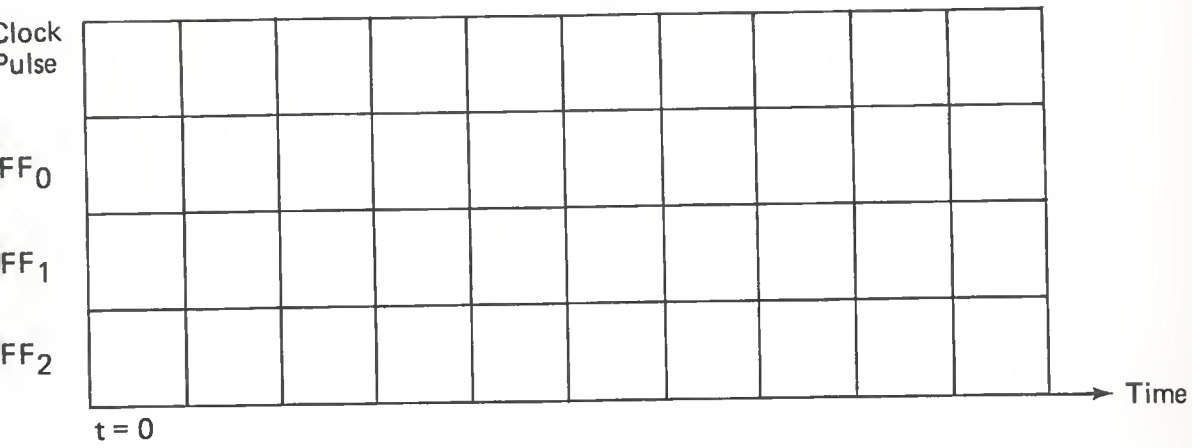


Fig. 19-8 The Data Tables

Pulse Train Data



Counting Data

Decimal Equivalent	CP	FF_2	FF_1	FF_0
0				
1	1			
2	1			
3	1			
4	1			
5	1			
6	1			
7	1			

Figure 19-8 The Data Tables (Cont'd)

EXPERIMENT 20 _____ Name _____

Date: _____ Class _____ Instructor _____

Truth Table		
t_n		$t_n + 1$
J	K	Q

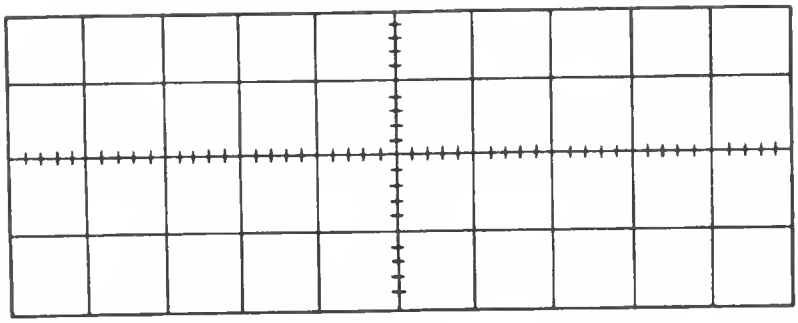
Ring Counter States							
Input	Reset	1	2	3	4	5	6
FF_0							
FF_1							
FF_2							
FF_3							
FF_4							
FF_5							

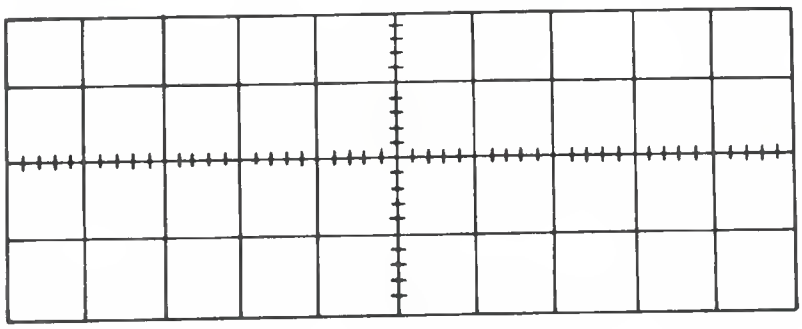
Effect of reset when count < 5 was _____

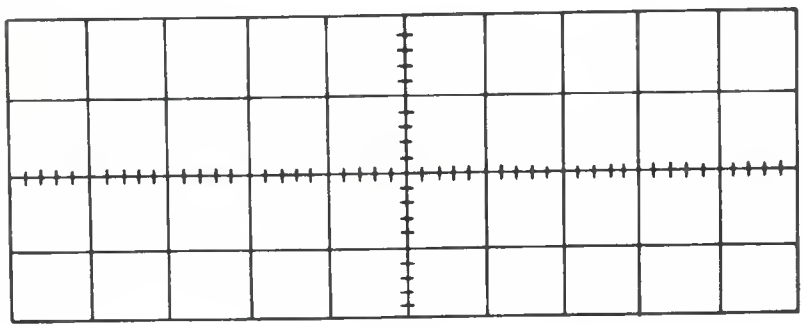
_____

_____

Fig. 20-4 The Data Tables







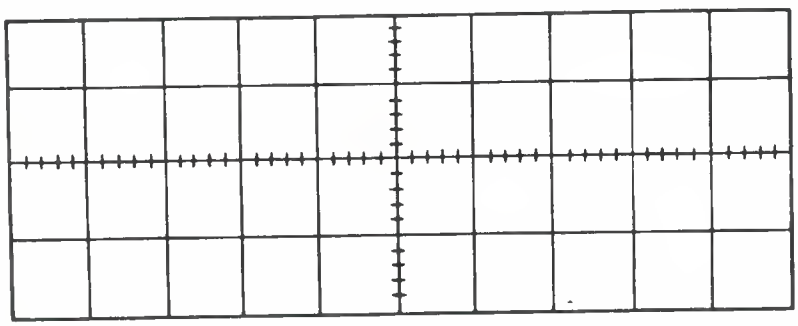
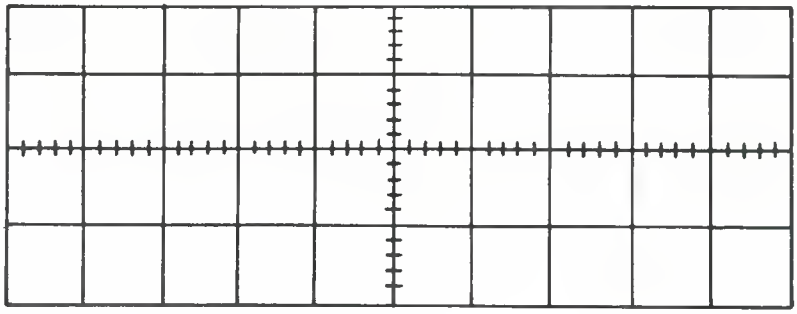
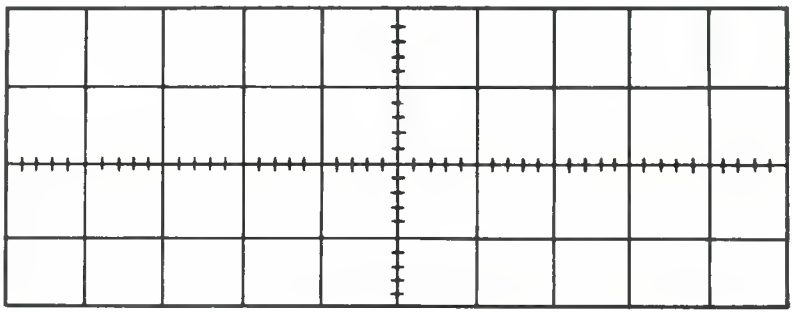
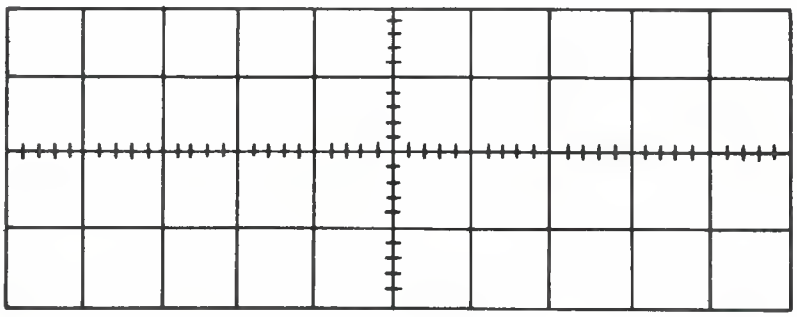


Fig. 20-4 The Data Tables (Cont'd)







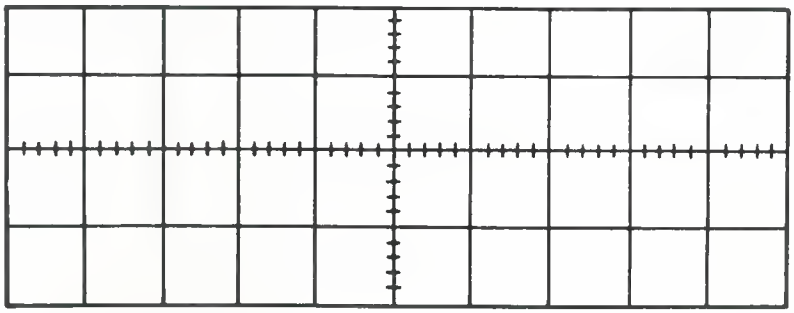
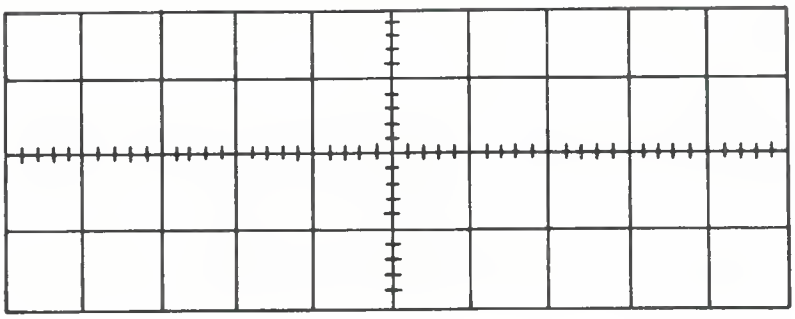
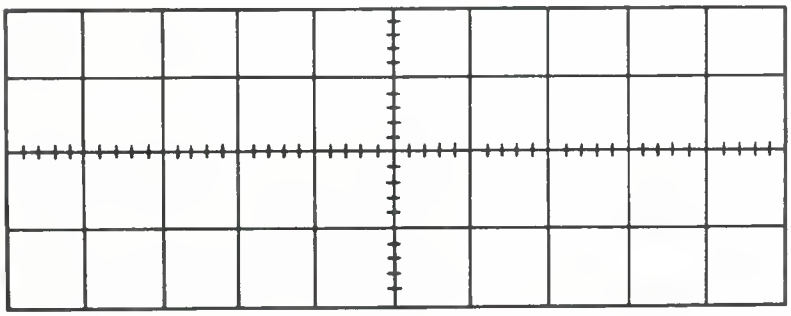
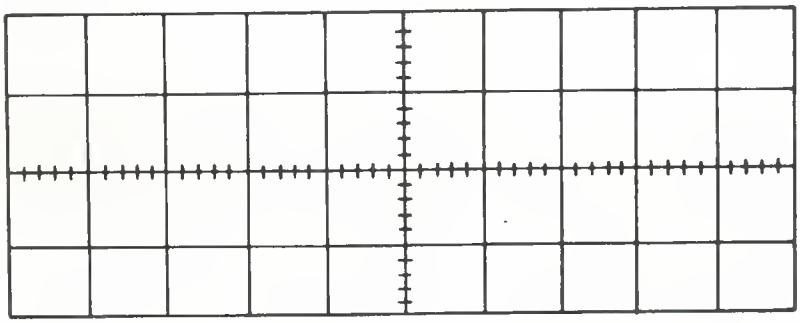


Fig. 21-12 The Results







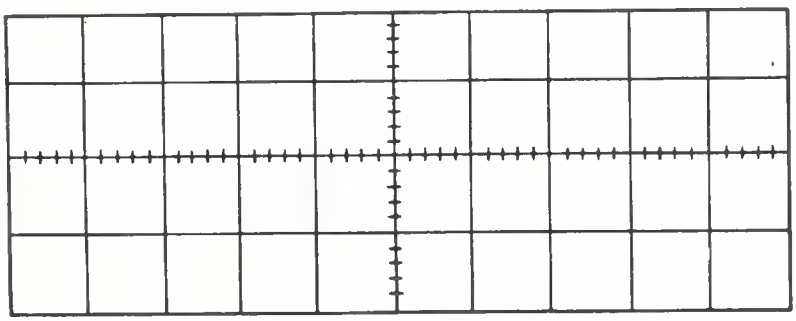


Fig. 21-12 The Results (Cont'd)

EXPERIMENT 22 _____ Name _____

Date: _____ Class _____ Instructor _____

Switch That is Closed	0		2^1		2^2		2^3	
	V		V		V		V	I
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								

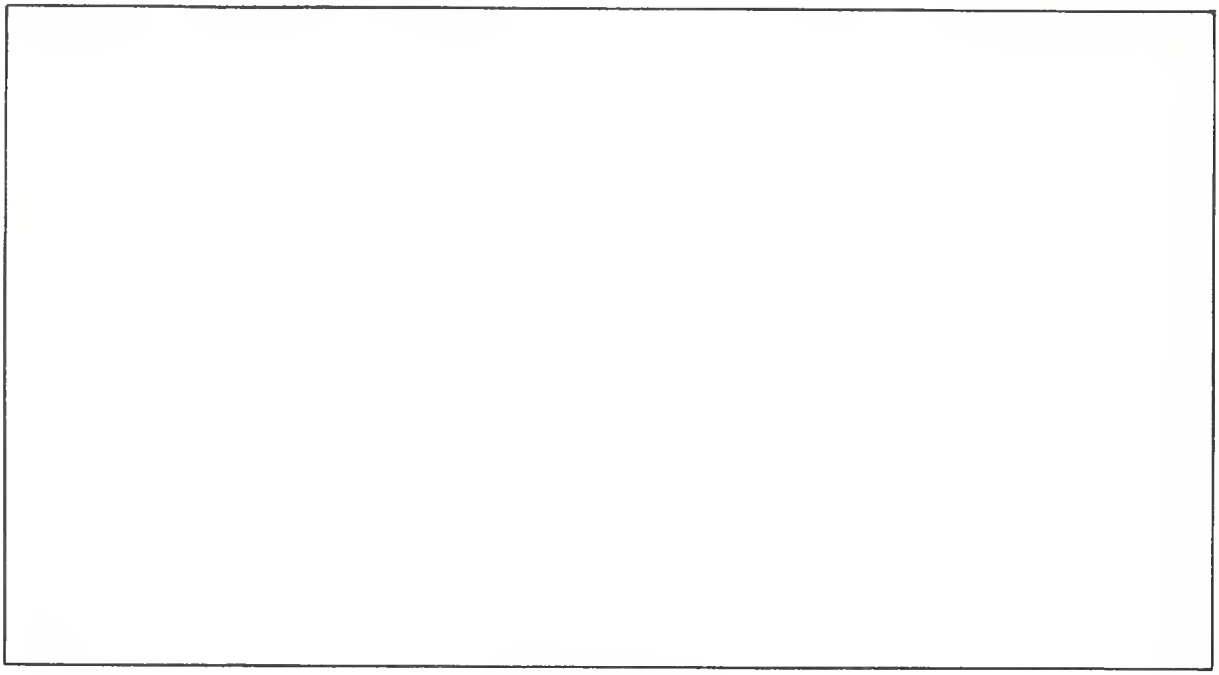
Voltage Level for 1 = _____

Voltage Level for 0 = _____

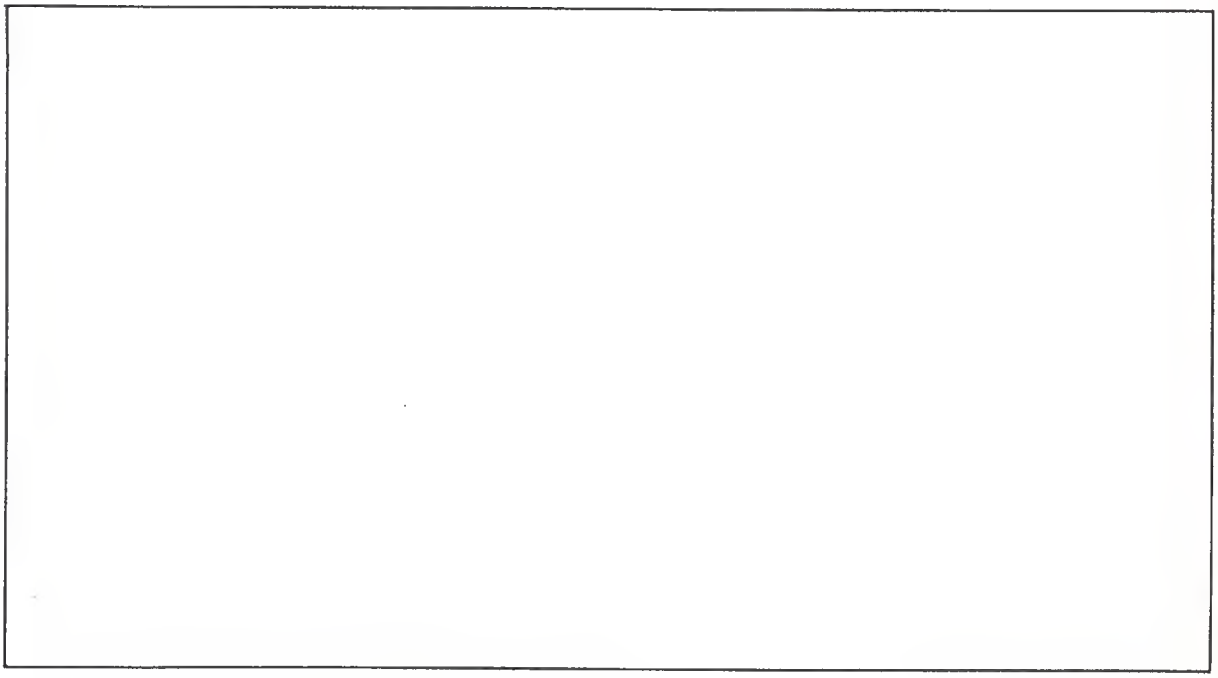
Fig. 22-6 The Data Table

EXPERIMENT 23 _____ Name _____

Date: _____ Class _____ Instructor _____

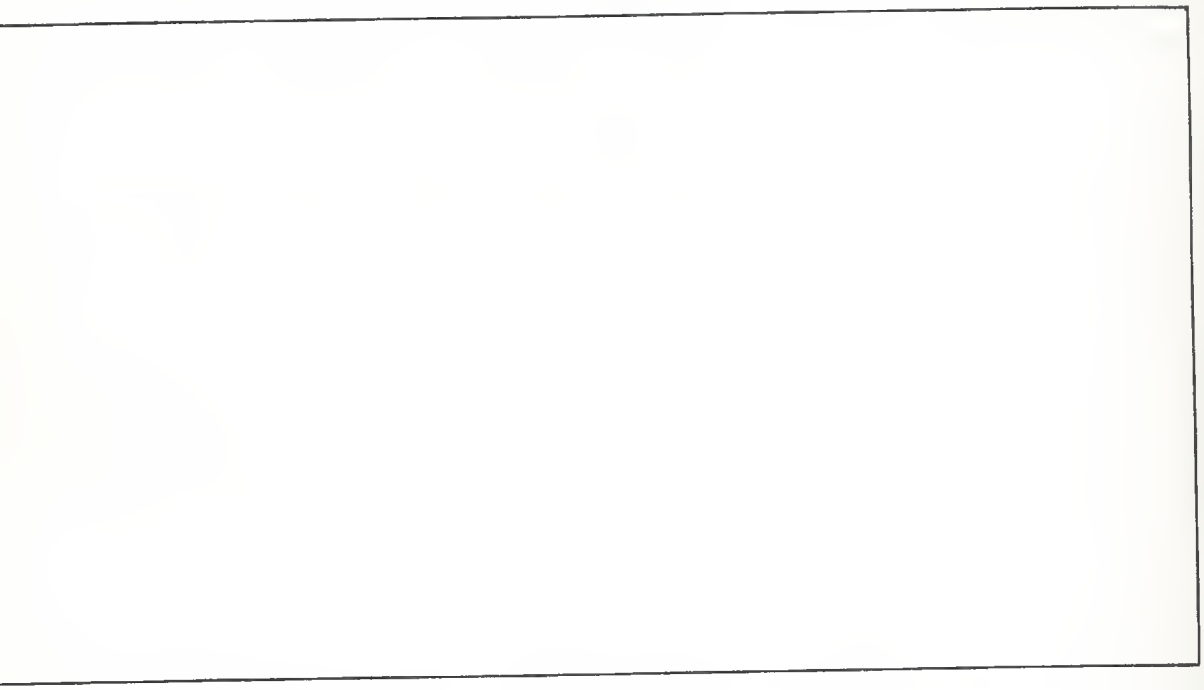


AND Gate

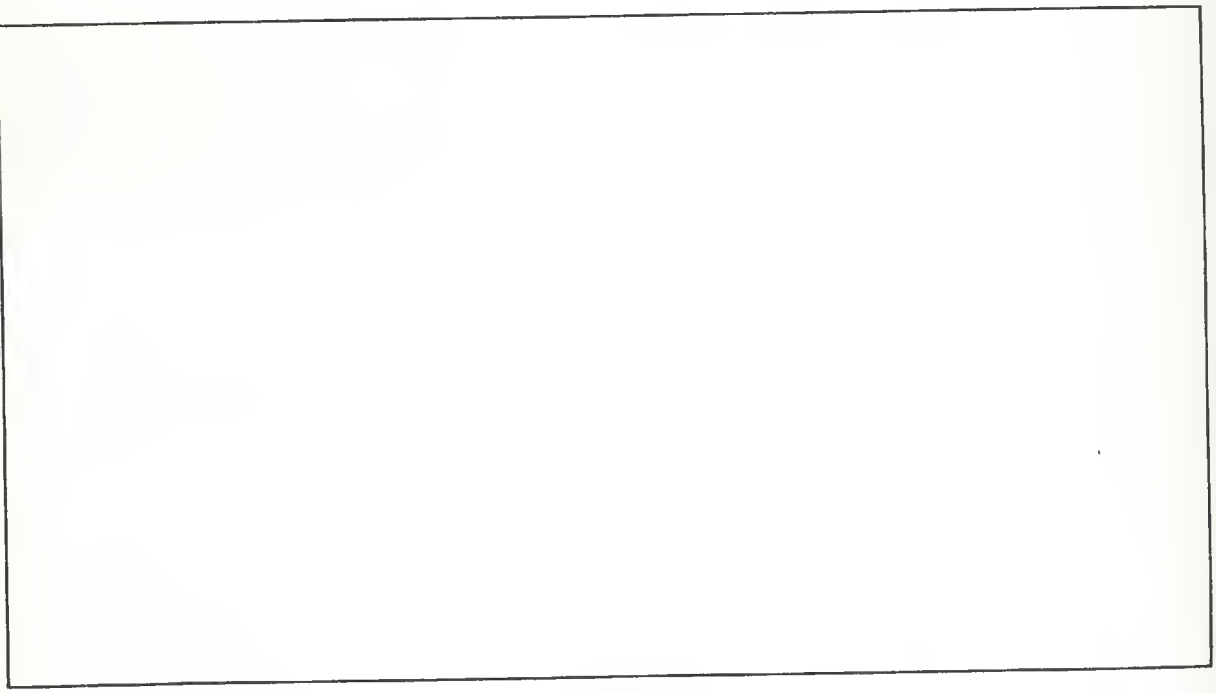


OR Gate

Fig. 23-3 Gate Diagrams



AND Gate

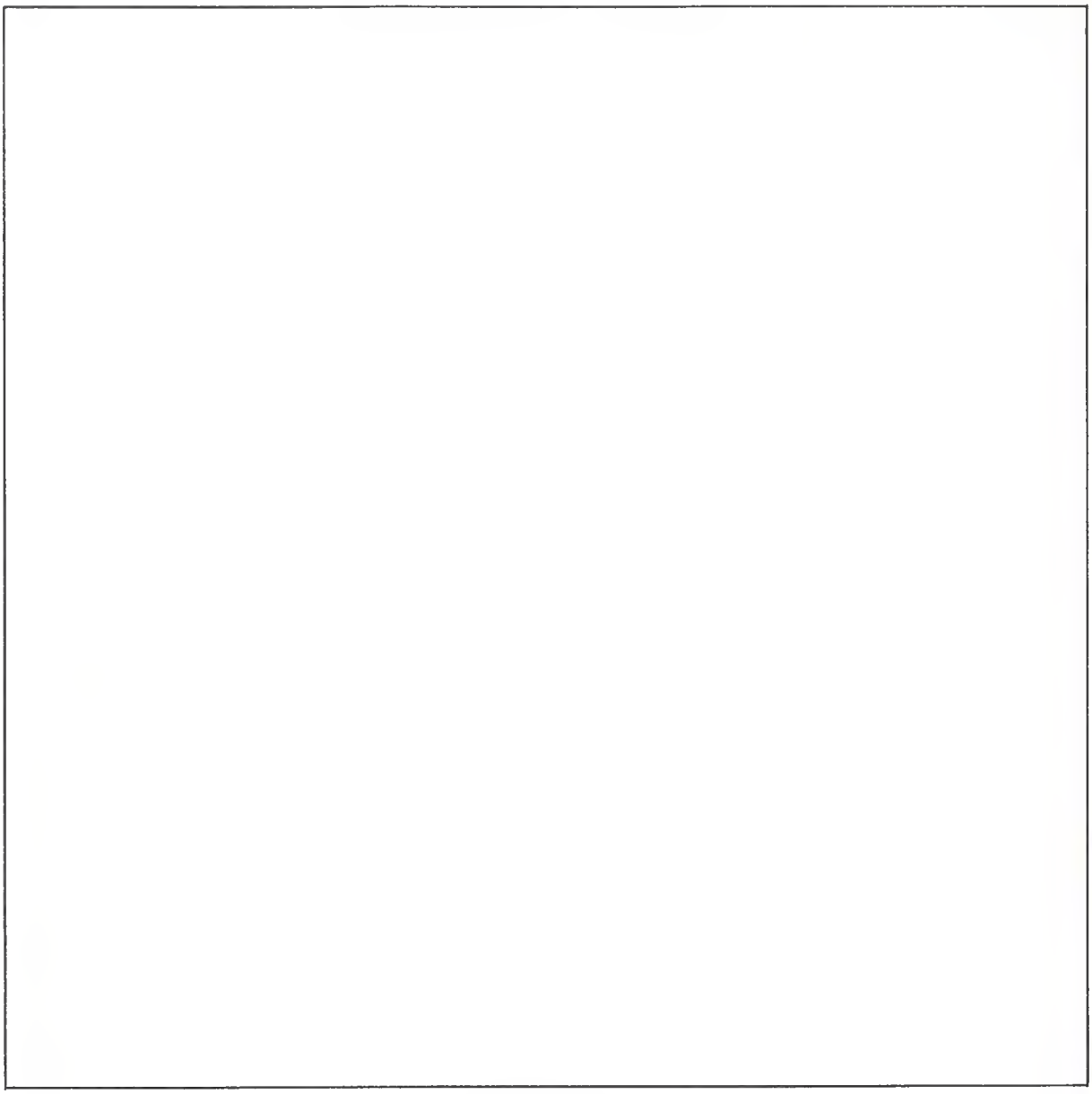


OR Gate

Fig. 23-3 Gate Diagrams (cont'd)

EXPERIMENT 23 _____ Name _____

Date: _____ Class _____ Instructor _____



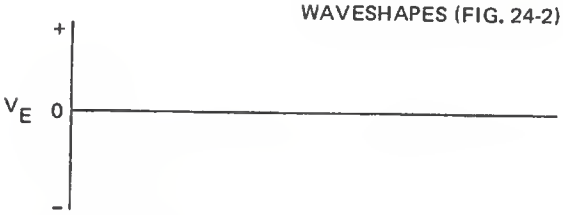
Truth Table

Fig. 23-4 The Truth Table

EXPERIMENT 24 _____ Name _____

Date: _____ Class _____ Instructor _____

WAVESHAPES (FIG. 24-2)



R_E	Calculated Frequency	Measured Frequency
1 kΩ		
2 kΩ		
4 kΩ		
8 kΩ		
10 kΩ		
12 kΩ		
14 kΩ		
16 kΩ		
18 kΩ		
20 kΩ		

Fig. 24-3 The Data Table

EXPERIMENT 25 _____ Name _____

Date: _____ Class _____ Instructor _____

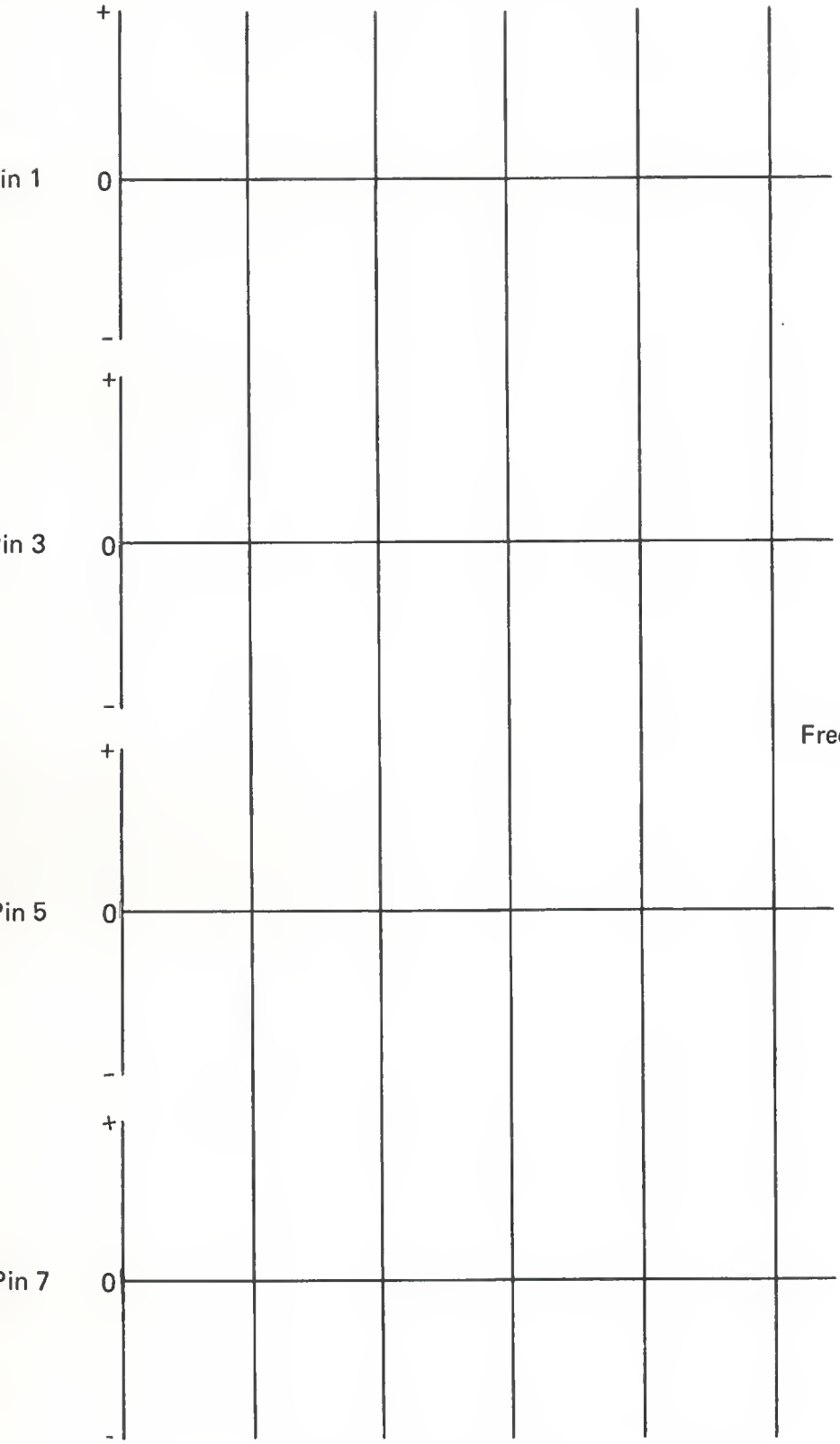
Input A (pin 1)	Input B (pin 2)	Output (pin 3)
0	0	
0	3.5	
3.5	0	
3.5	3.5	

(A)

A	B	Output
0	0	
0	1	
1	0	
1	1	

(B)

Fig. 25-6 Data for the NOR Logic



Frequency =_____ Hz

Fig. 25-7 Data Table for Multivibrator

EXPERIMENT 26 _____ Name _____

Date: _____ Class _____ Instructor _____

Time	Thermistor Resistance	Temperature
10 sec		
30 sec		
50 sec		
60 sec		
2 min		
3 min		

Fig. 26-4 The Data Table

EXPERIMENT 27 _____ Name _____

Date: _____ Class _____ Instructor _____

BINARY				DECIMAL
$(d)2^3$	$(c)3^2$	$(b)2^1$	$(a)2^0$	
0	0	0	0	0
				1
				2
				3
				4
				5
				6
				7
				8
				9
				10
				11
				12
				13
				14
				15

Fig. 27-6 The Data Tables

BINARY				DECIMAL
$(d)2^3$	$(c)2^2$	$(b)2^1$	$(a)2^0$	
0	0	0	0	0
				1
				2
				3
				4
				5
				6
				7
				8
				9
				10
				11
				12
				13
				14
				15

Fig. 27-6 The Data Tables (Cont.)

378000